ahead of Change
hynix

Good memory

Key Success Factor of SSD

Hynix Semiconductor Inc.

Oct. 20, 2008

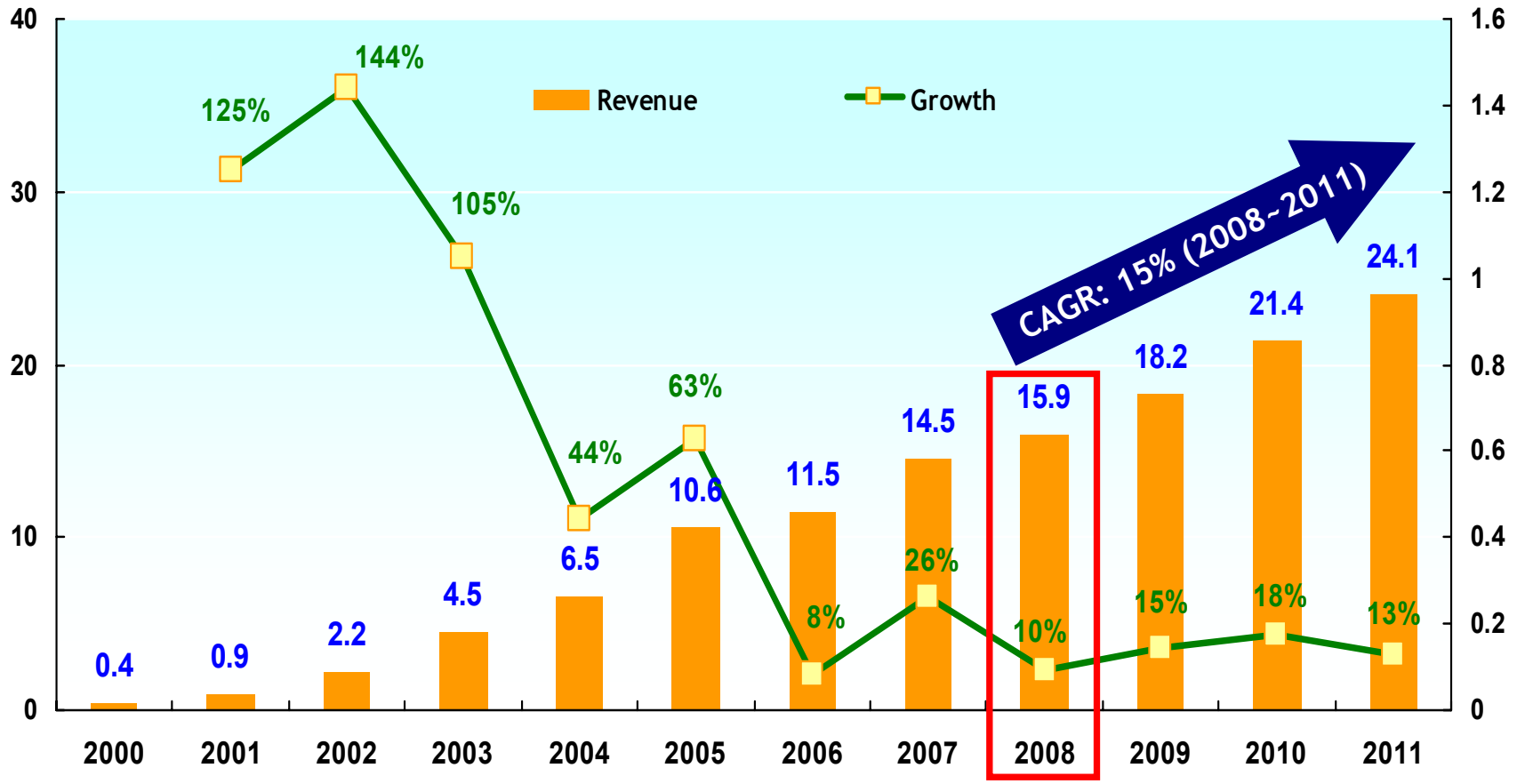
Presentation Agenda

1. **Market Introduction**
2. Key Success Factor
   - Raw NAND
   - Performance & Reliability
3. Conclusion

NAND Market Forecast: Overall

Slower but Continuous Growth in NAND Market from 2008

Unit : B$



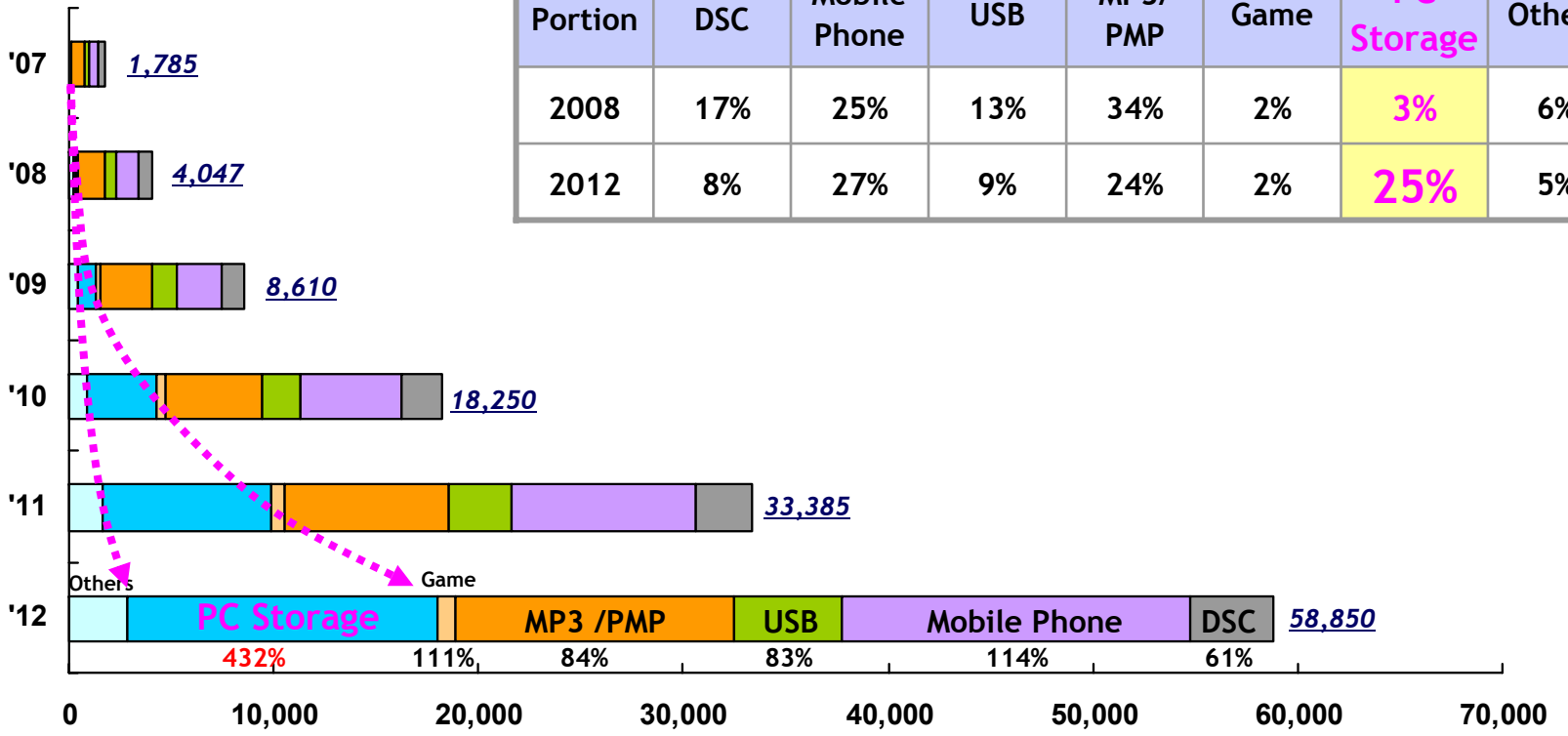
Source : WSTS

NAND Application Trend

Strong & Continuous Demand from PC Storage

Unit : Mpcs (8Gb EQ)

Portion	DSC	Mobile Phone	USB	MP3/ PMP	Game	PC Storage	Others
2008	17%	25%	13%	34%	2%	3%	6%
2012	8%	27%	9%	24%	2%	25%	5%



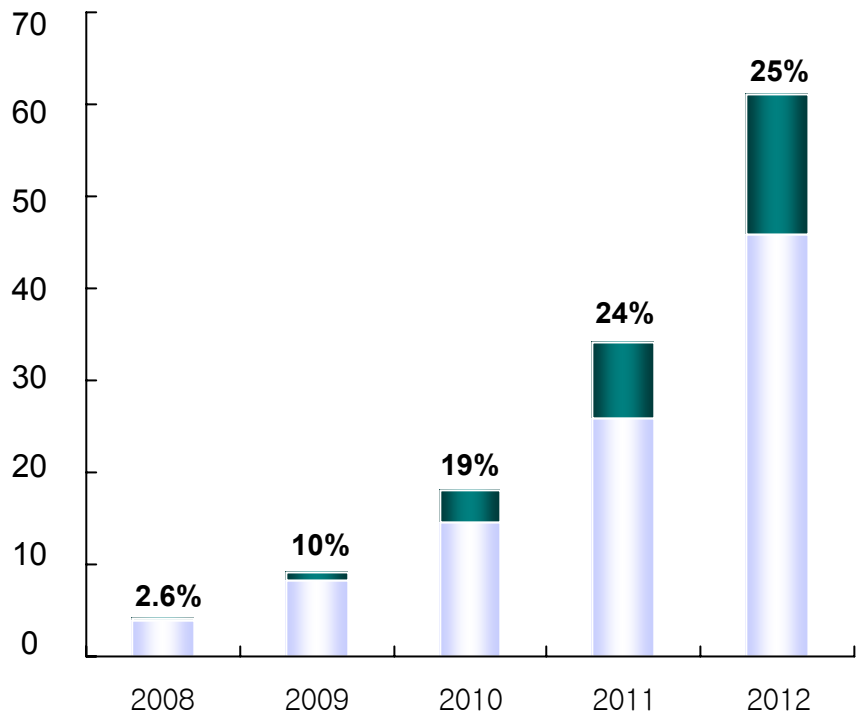
Source : Hynix Marketing

SSD Market Forecast

PC will be a new killer application of NAND

PC Portion in NAND Market

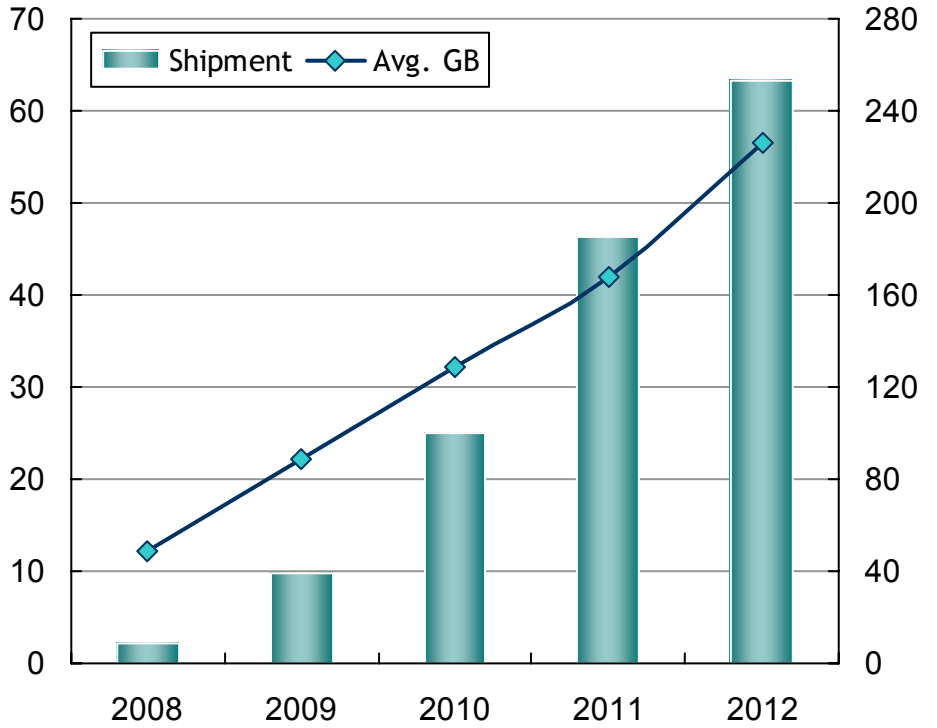
Unit : Bpcs (8Gb EQ)



SSD Market Forecast

Unit : Mpcs

Unit : GB

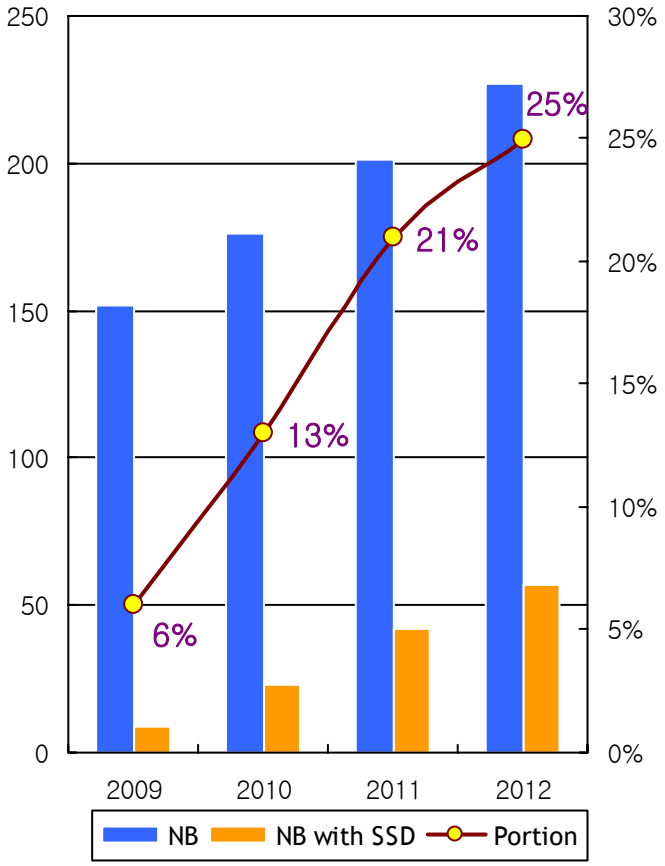


Source : Hynix Marketing

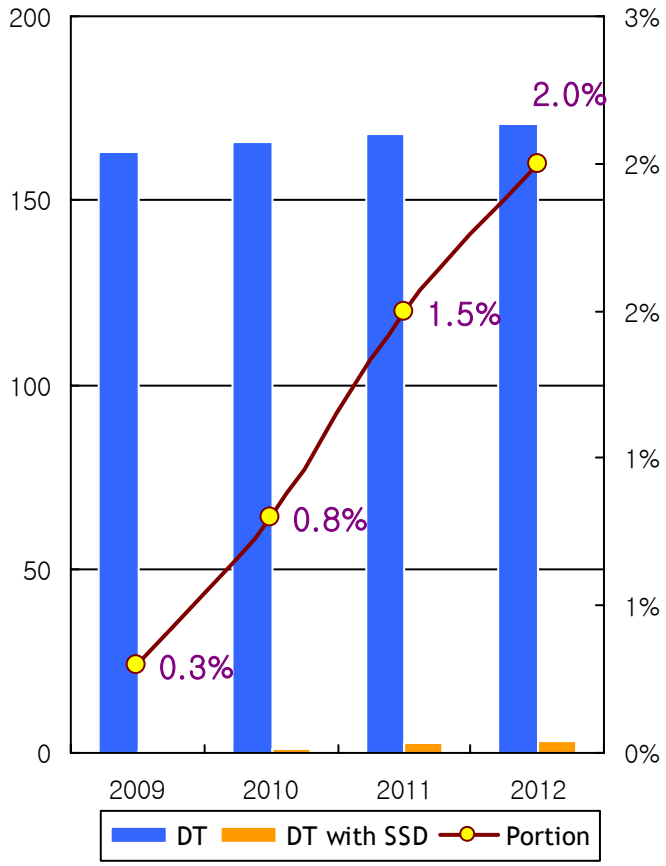
SSD Adoption Rate in Computing Device

Unit : Mpcs

[Notebook]



[Desktop]



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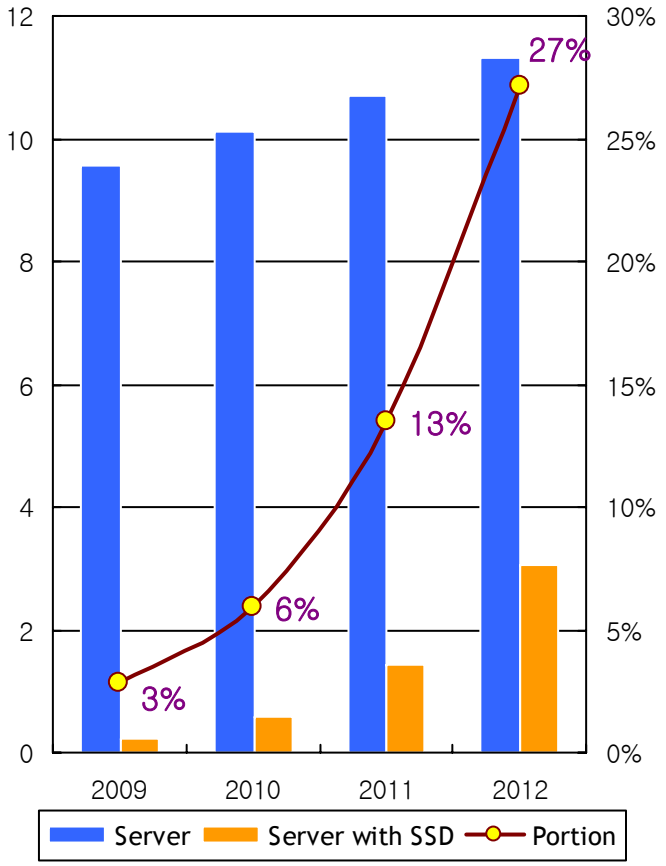
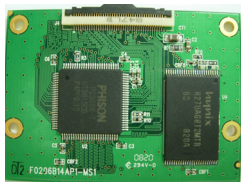


Source : Hynix Marketing

SSD Market Segmentation

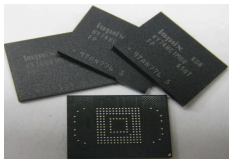
[HDD Type]

- I/F: SATA 3Gbps
- Size: 1.8”, 2.5”
- Density: 256GB in 2009



[Module Type]

- I/F: PATA, SATA
- Size: Customized
- Density: 64GB in 2009



[Chip Type]

- I/F: eMMC
- Size: 14 x 18 x 1.3 mm, 169FBGA
- Density: 32GB in 2009

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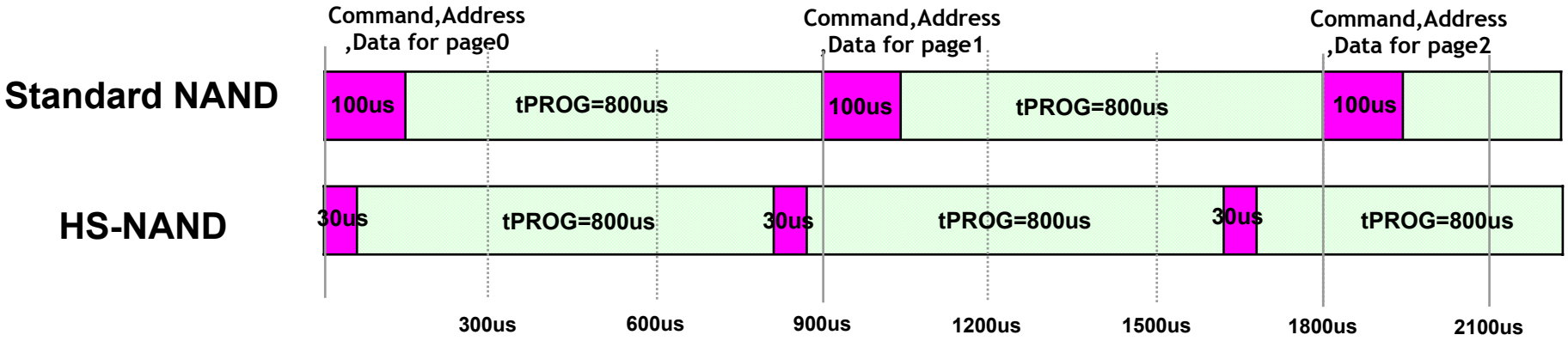
NAND Performance Comparison

	Standard NAND (SLC)	Standard NAND (MLC)	HS-NAND (MLC)	Remark
Read Performance	38MB/sec	38MB/sec	112MB/sec	2Plane with Interleave + 2CE
Write Performance	38MB/sec	16MB/sec	19MB/sec	2Plane with Interleave + 2CE

Standard NAND: tPROG=200us(SLC)/800us(MLC), tRC/tWC=25ns, tR=25us(SLC)/50us(MLC)

HS-NAND : tPROG=800us(MLC), tRC/tWC=7.5ns, tR=50us



Comparison between HS NAND and STD NAND

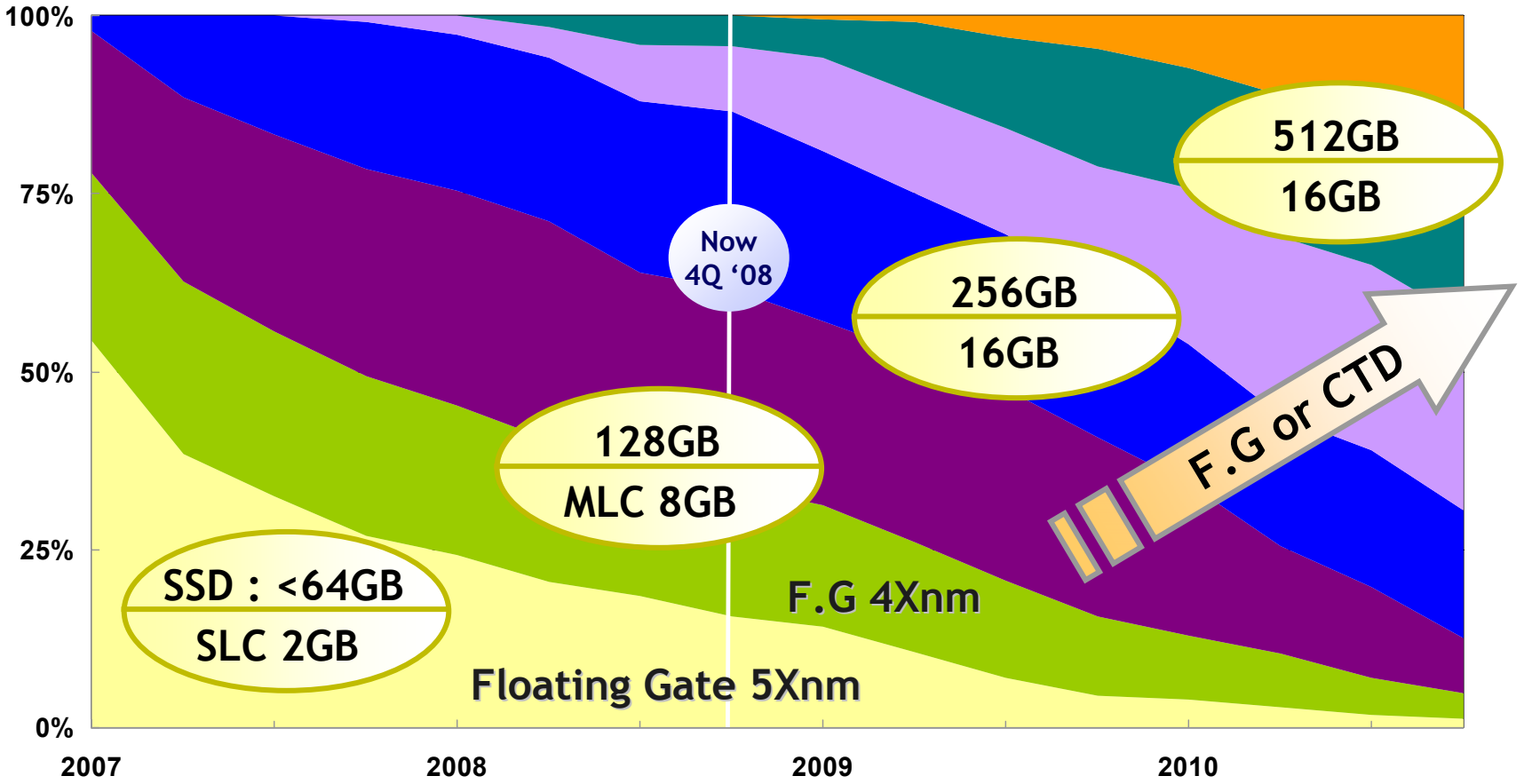
- Interface Speed
  - Cycle time(tRC/tWC) is important for NAND performance
  - Maximize the performance using by high speed interface scheme

    ➔ HS-NAND (High speed NAND, DDR)

Standard NAND (ONFI 1.0)	Feature	HS-NAND (ONFI 2.0)
No	Synchronous Interface	Yes
≥ 25ns (SDR)	tRC/tWC	7.5ns (DDR)
No	Scalable Higher Performance	Yes
Some	Cache Mode	Yes
2.7V ~ 3.6V	VCCq	1.7V ~ 1.95V
2.7V ~ 3.6V	VCC	2.7V ~ 3.6V

Migration for NAND Cell structure

CTD will be one of solution for <3xnm NAND



Source : Hynix Marketing

Characteristics of CTD Technology

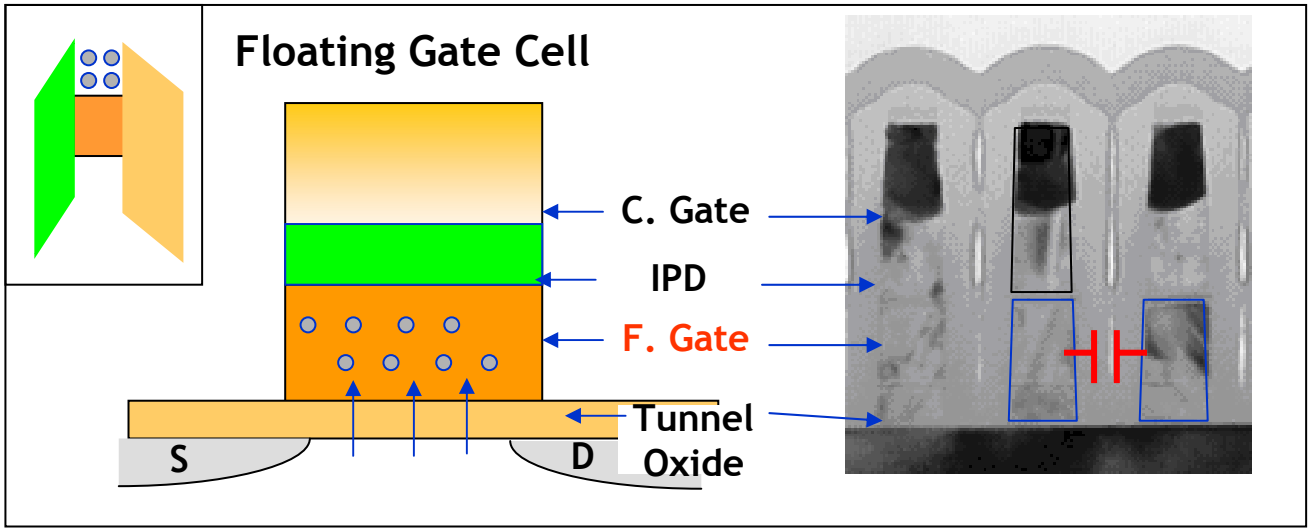
What are the critical issues?

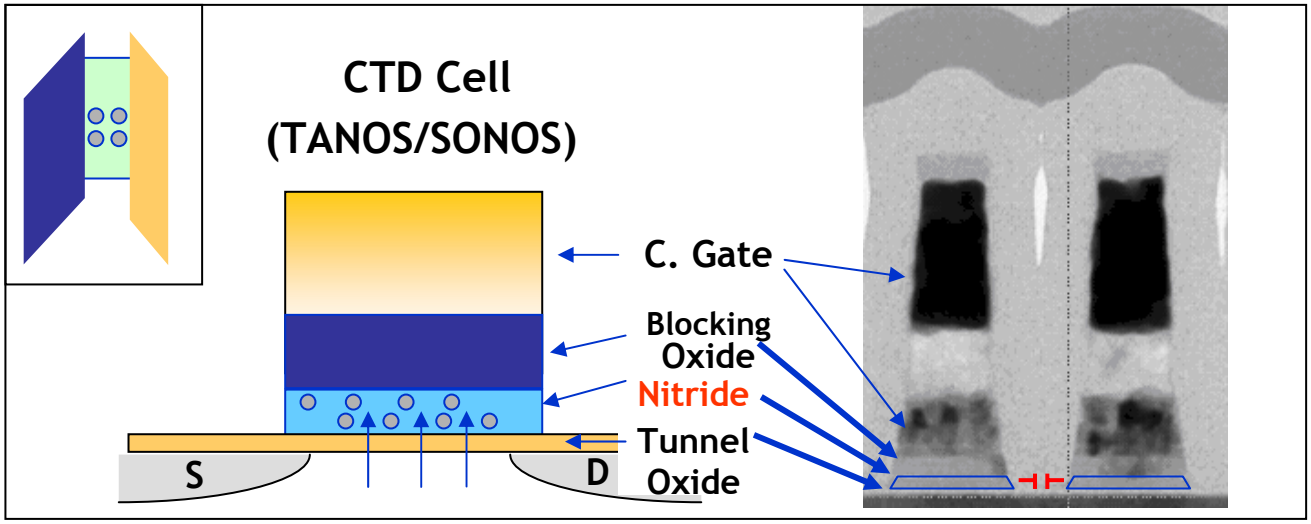
- Floating gate spacing limitation; ~35nm
- Cell to cell interference
- Retention

➔ CTD (Charge Trap Device)

Introduction to CTD

Structure & X-section





Material

Control Gate	Poly-silicon
IPD (ONO)	Top Oxide/Nitride / Bottom Oxide
Floating Gate	Poly-silicon (Free Electron)
Tunnel Oxide	Thermal Oxide

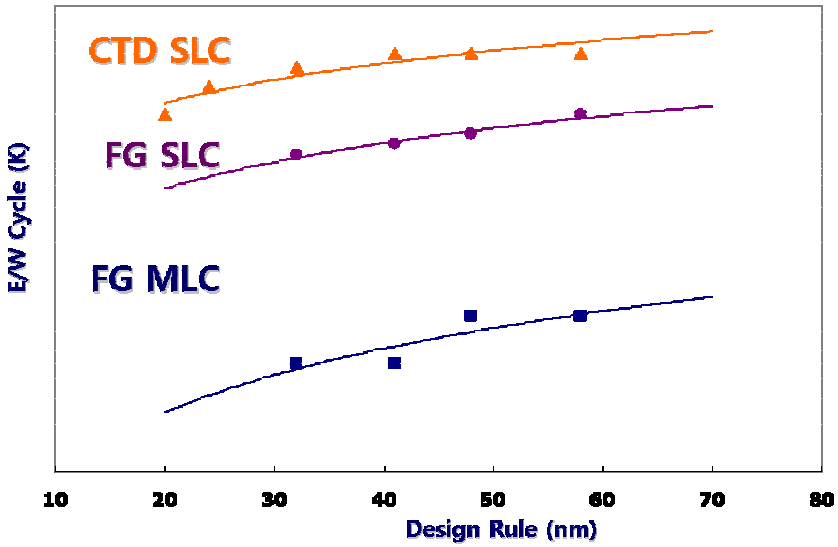
Control Gate	Metal Gate
Blocking Oxide	High-K Dielectric
Charge Trap	Nitride (Trapped electron)
Tunnel Oxide	Thermal Oxide

Electrical Characteristics of CTD

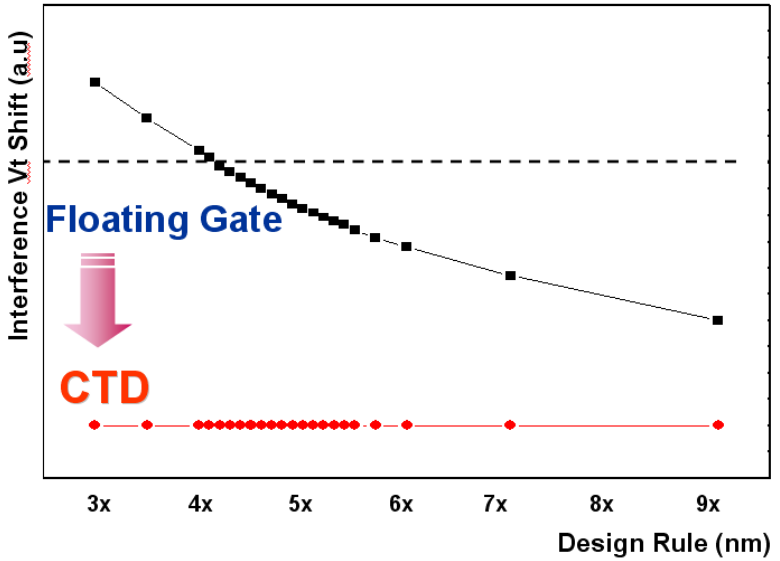
Better E/W Characteristics

Less Interference

than FG NAND



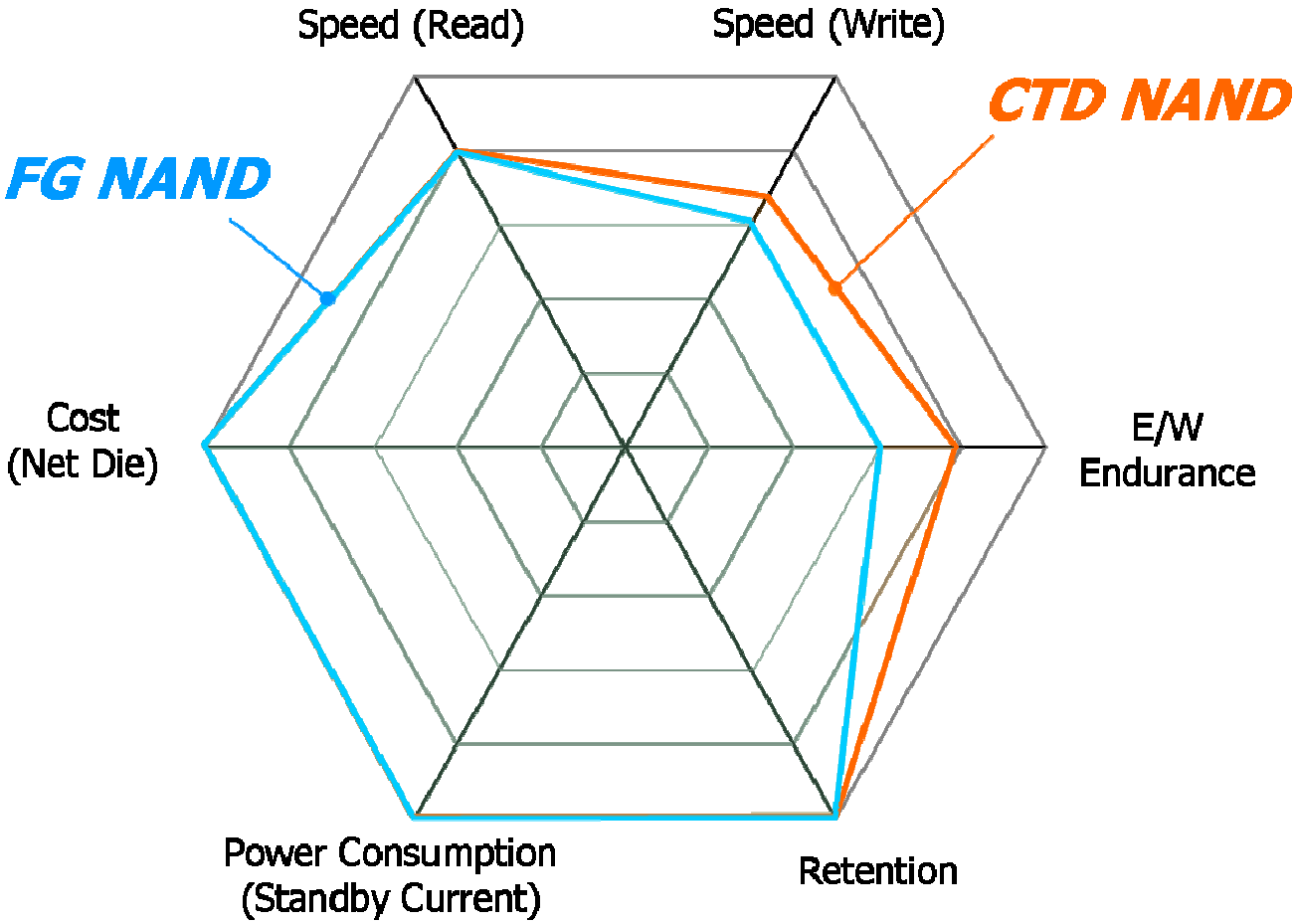
E/W Cycling Characteristics



Cell-to-Cell Interference

Advantages of CTD

CTD will drive Flash-SSD technology



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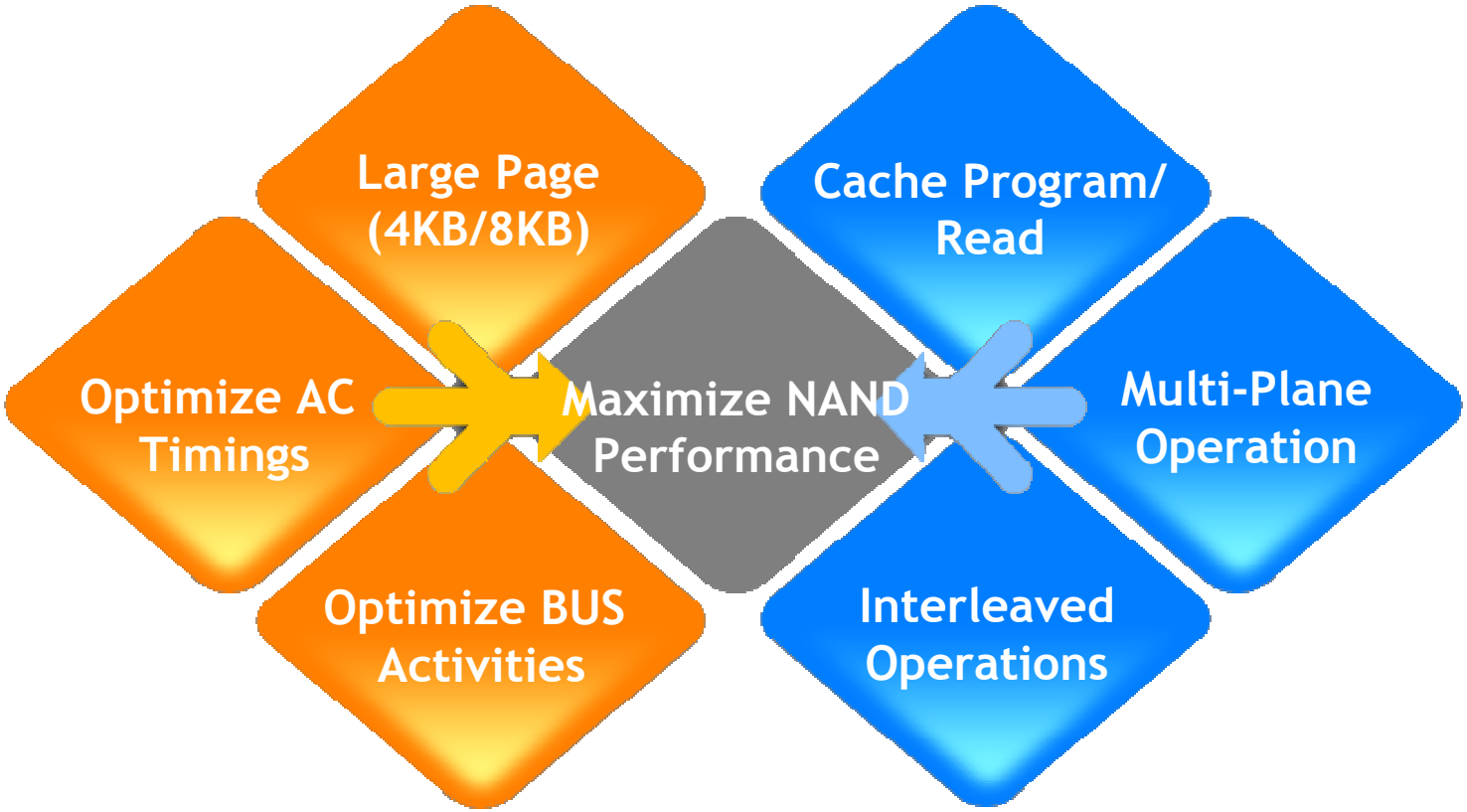
Factors to enhance NAND performance - I

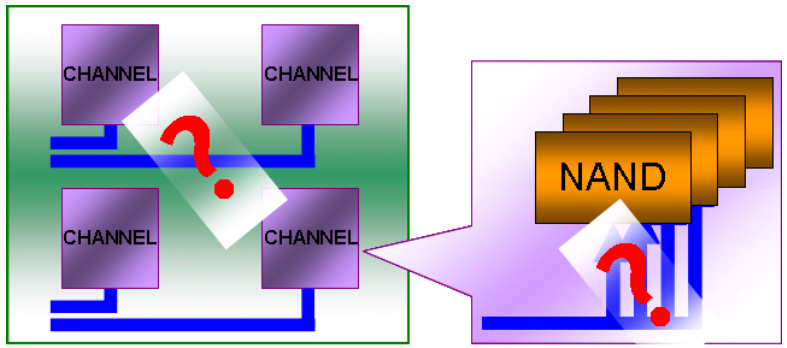
- **Performance can be enhanced by key parameters**

  (Multi chip operation, Larger page device, Cache Program/Read, etc)



Factors to enhance NAND performance - II

- ✓ How to enhance the NAND performance ?
  - *Multi-channel, Multi-way interleaving parallelism.*



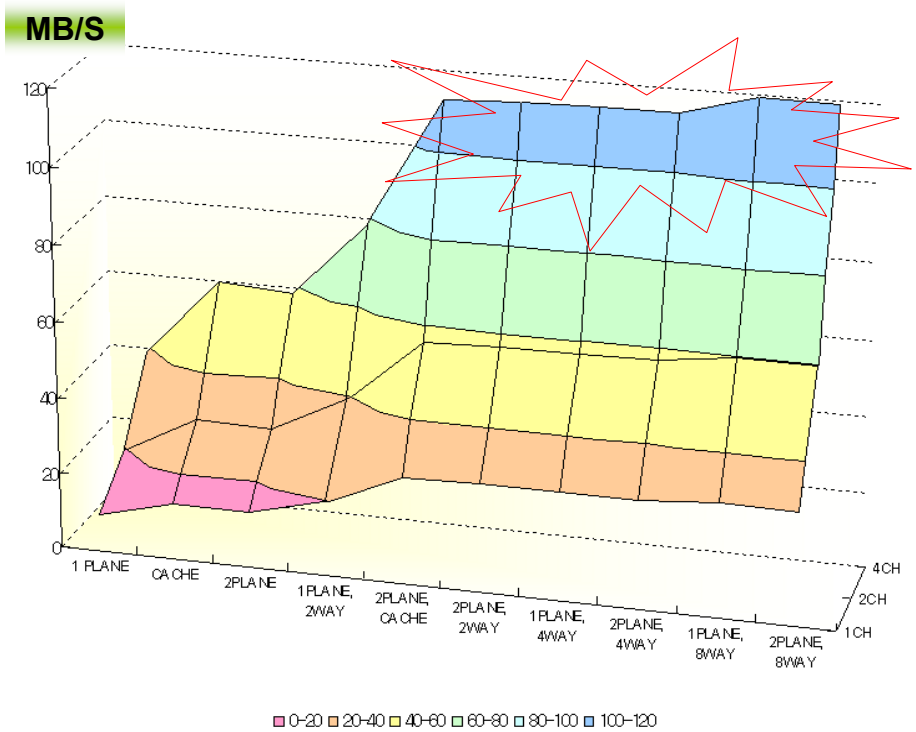
SLC → PAGE SIZE : 4K, tWC : 25ns, tPROG : 200us

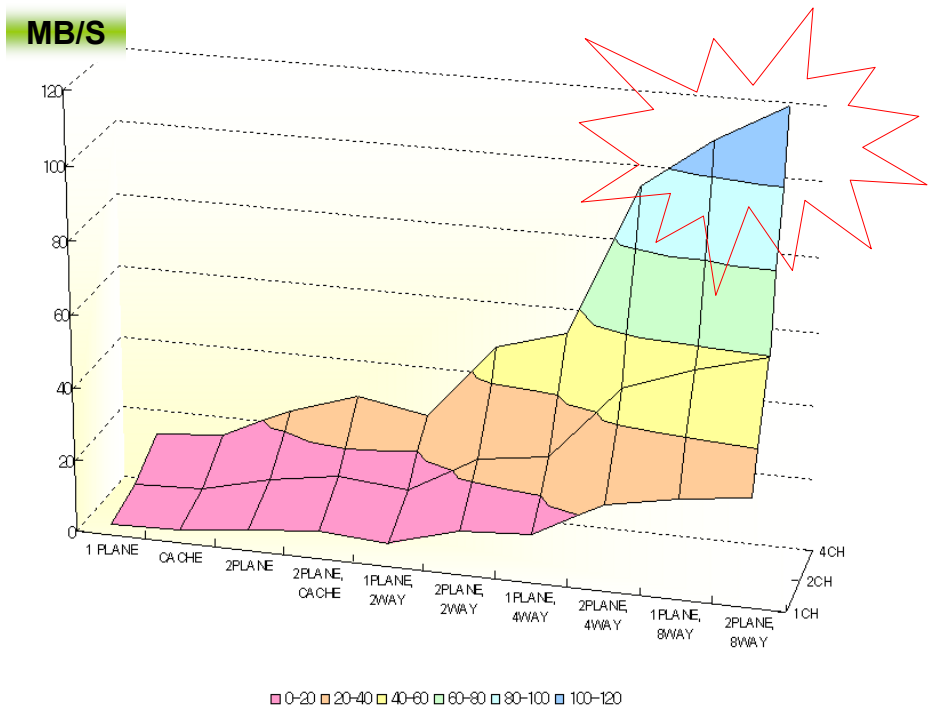
MLC → PAGE SIZE : 4K, tWC : 25ns, tPROG : 800us

UNIT [MB/S]

CHANNEL		1PLANE	CACHE	2PLANE	1PLANE 2WAY	2PLANE CACHE	2PLANE 2WAY	1PLANE 4WAY	2PLANE 4WAY	1PLANE 8WAY	2PLANE 8WAY
1	SLC	9.8	14.9	14.6	19.6	28.1	28.4	28.4	28.5	29.8	29.8
	MLC	3.3	3.7	5.9	6.6	7.5	11.9	13.3	23.7	27.1	29.8
2	SLC	19.6	29.8	29.2	39.2	56.2	56.8	56.8	57	59.6	59.6
	MLC	6.6	7.4	11.8	13.2	15	23.8	26.6	47.4	54.2	59.6
4	SLC	39.2	59.6	58.4	78.4	112.4	113.6	113.6	114	119.2	119.2
	MLC	13.2	14.8	23.6	26.4	30	47.6	53.2	94.8	108.4	119.2

Performance Data

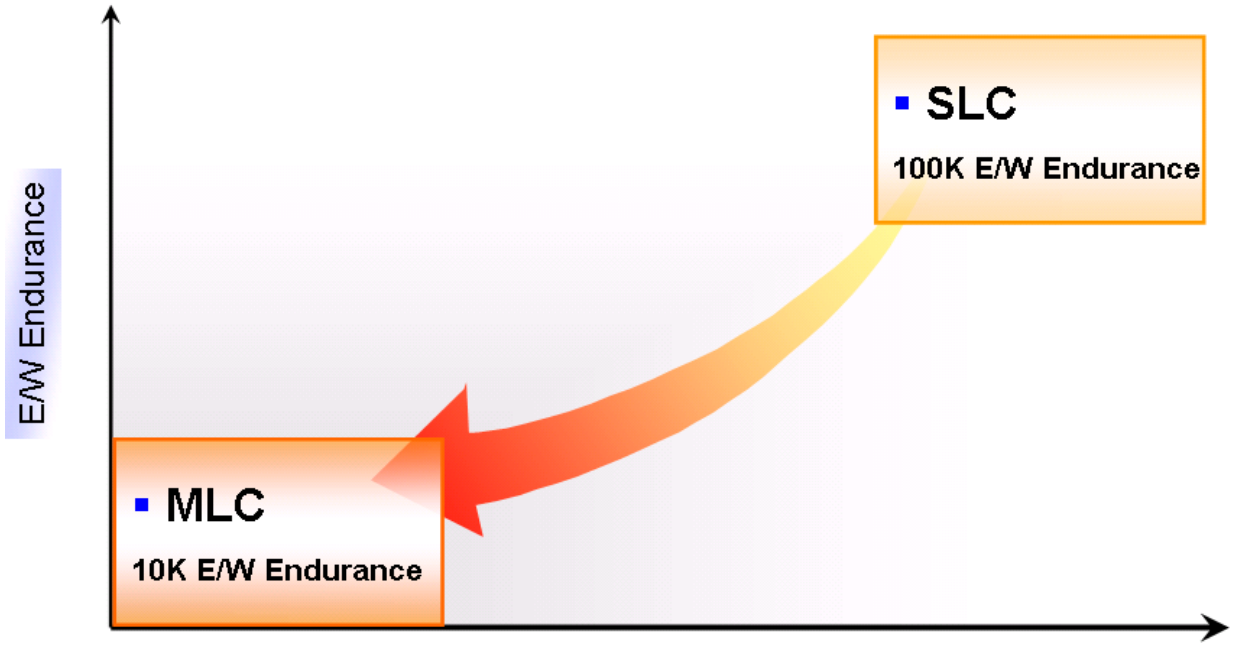




- ✓ SLC
  - Page Size : 4KB
  - tWC : 25ns
  - tPROG : 200us
- ✓ MLC
  - Page Size : 4KB
  - tWC : 25ns
  - tPROG : 800us

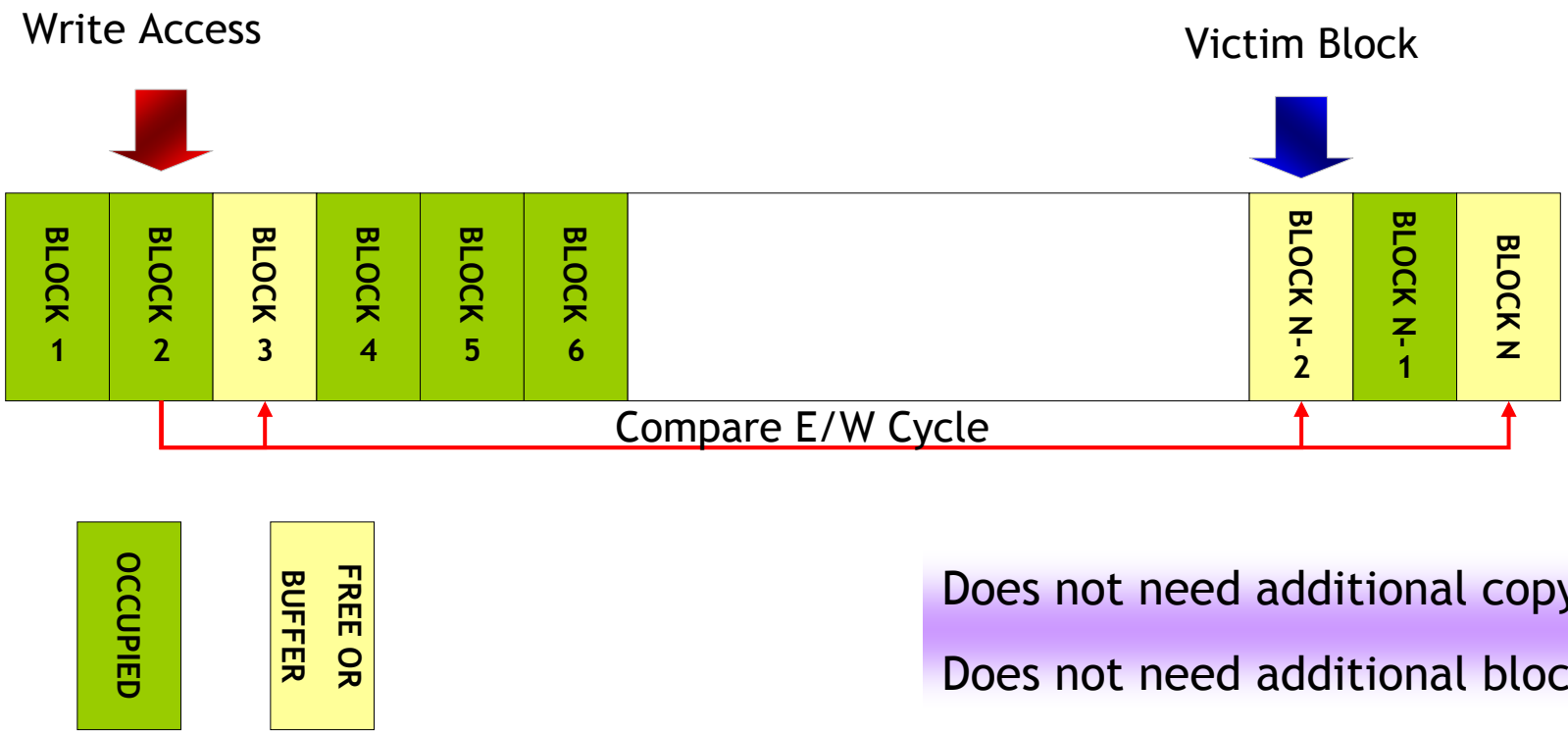
Introduction of Wear-leveling - I

- ✓ E/W endurance is related with tech and type of cell.
- ✓ Tech. shrink cause to lower E/W performance, so optimal wear-leveling must be required.



Introduction of Wear-leveling - II

- ✓ **Dynamic Wear Level**
- ✓ Static Wear Level
- ✓ Global Wear Level



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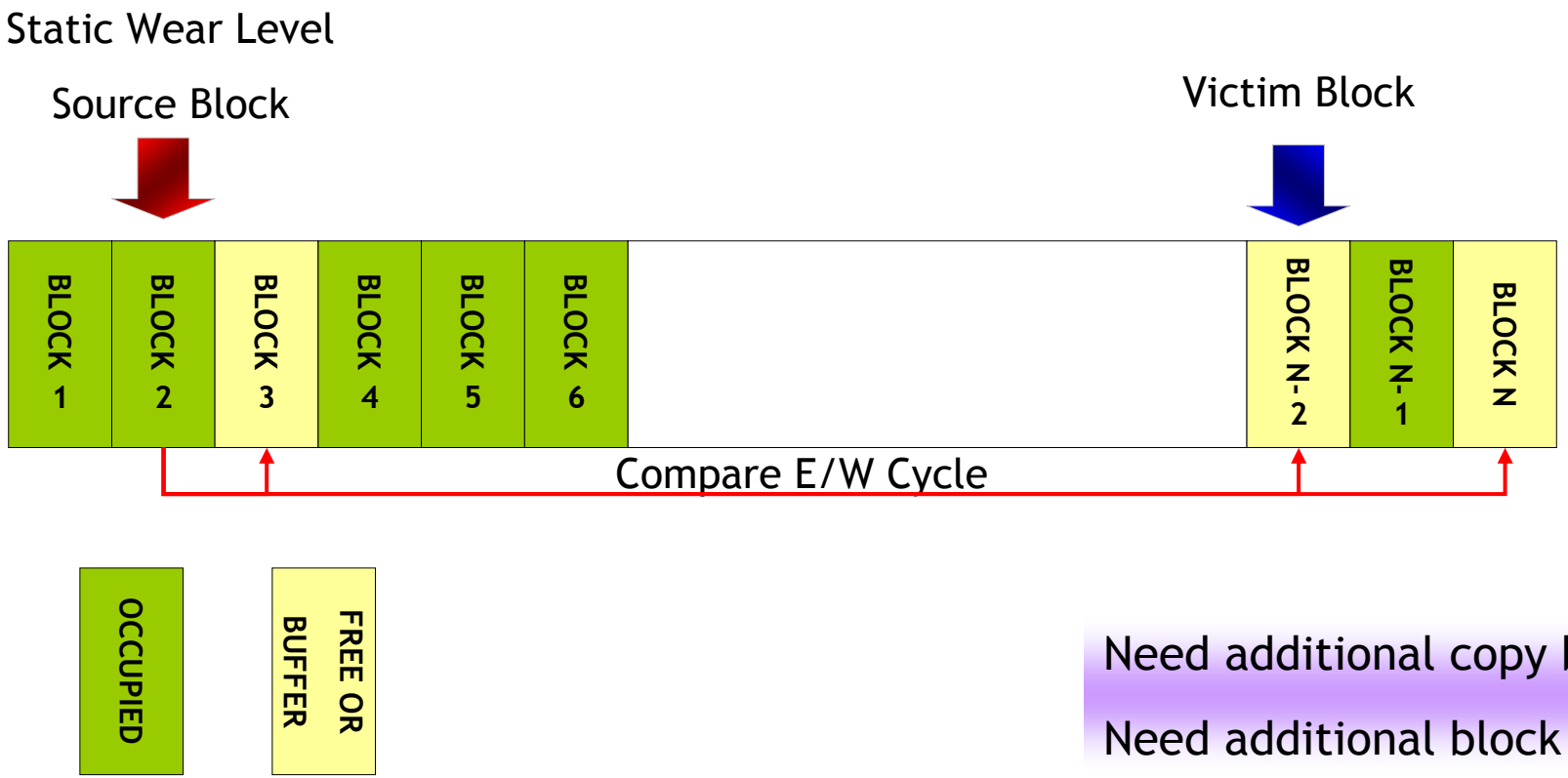
Does not need additional block erase

Introduction of Wear-leveling - III

- ✓ Dynamic Wear Level
- ✓ **Static Wear Level**
- ✓ Global Wear Level



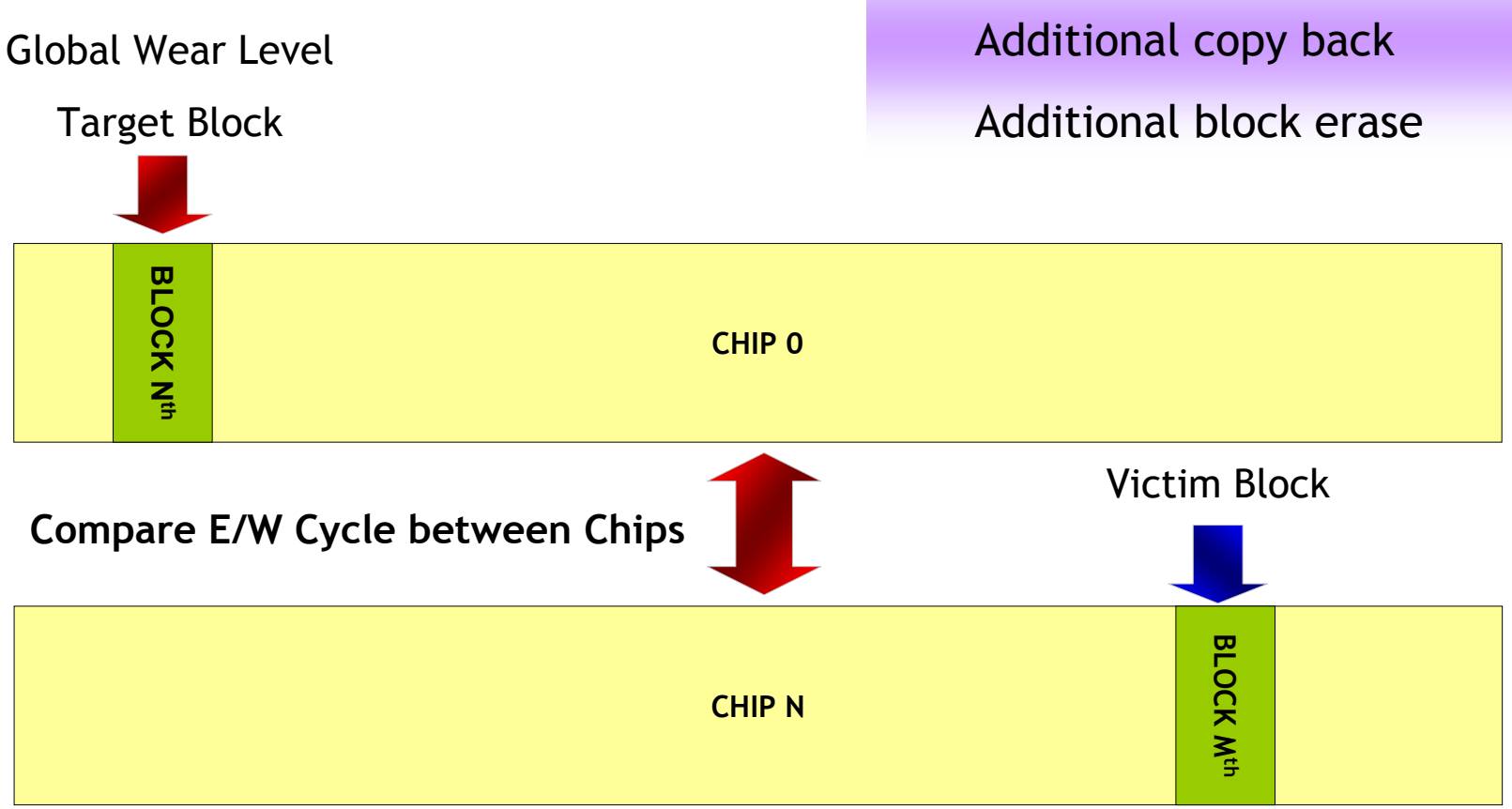
Introduction of Wear-leveling - IV

- ✓ Dynamic Wear Level
- ✓ Static Wear Level
- ✓ **Global Wear Level**

Every global wear level cause

Additional copy back

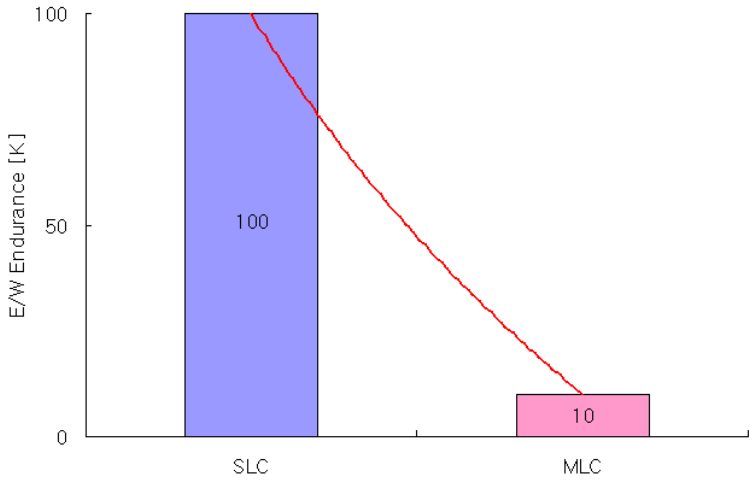
Additional block erase

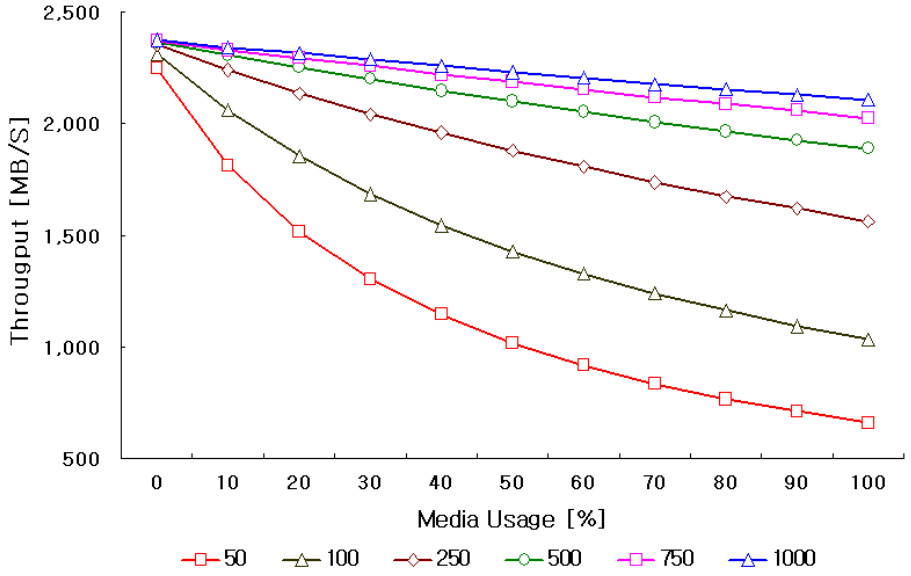


Performance trade-off by Wear-leveling

Frequent wear leveling may degrade performance

➔ *Additional E/W cycle + Read out & Write back*





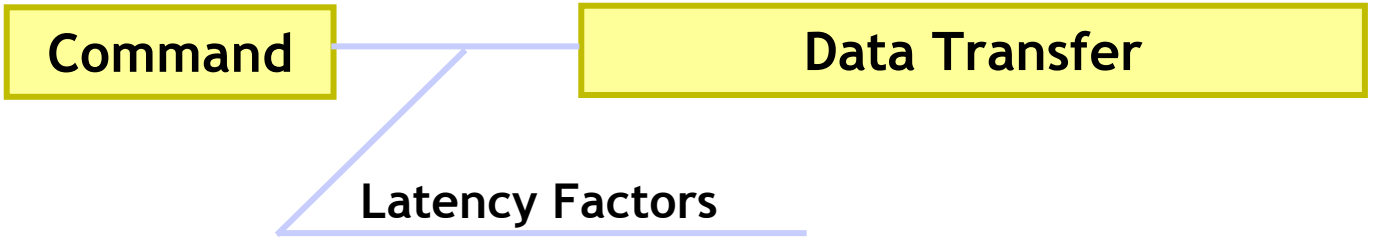
Wear level threshold

Good memory

Advanced Controller (Hardwired-FTL)

Software based FTL causes Long latency

➔ Reduced by Hardwired FTL



Latency Factors

- Address transition
- Map table Look-up
- Define write buffer policy; Random or Sequential
- (Channel 1)
- Data transfer
- (Channel 2)
- Data transfer
- (Channel 3)
- …

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Conclusion

- Limitation of current FG technology should be resolved by adopting new technology(CTD)
- High Speed interface enhances the performance
- Optimal Wear-leveling algorithm satisfying both Performance and Reliability
- Complexities of NAND Management require Hard-wired FTL design

Thank You !!!