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Wear Leveling for TLC NAND Flash

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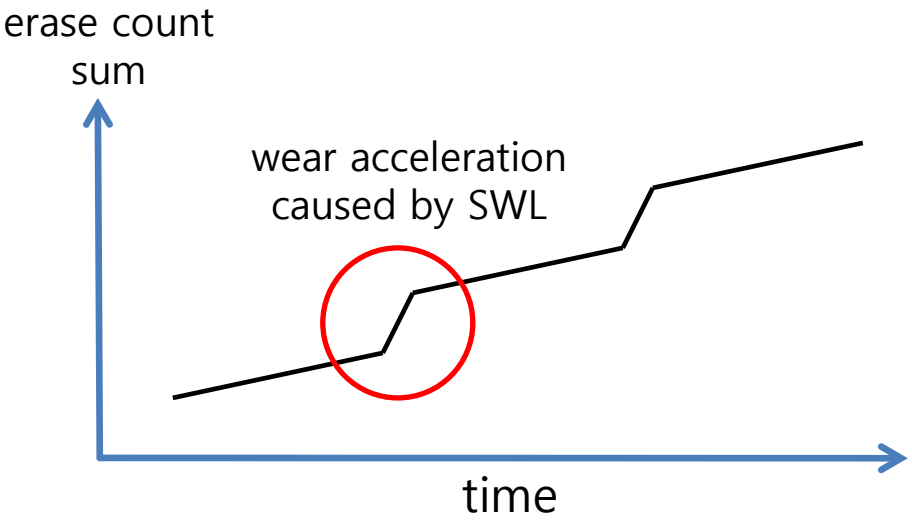
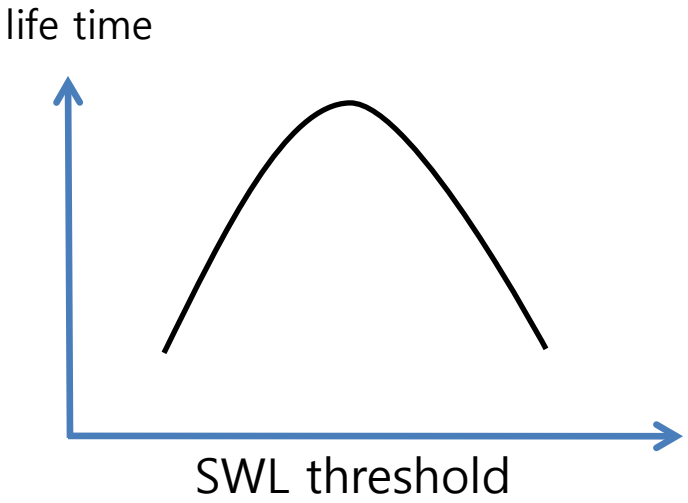
Agenda

- Impact of Static Wear Leveling
- Impact of Over Provisioning
- Impact of Global Wear Leveling
- Miscellaneous Issues

Impact of Static Wear Leveling

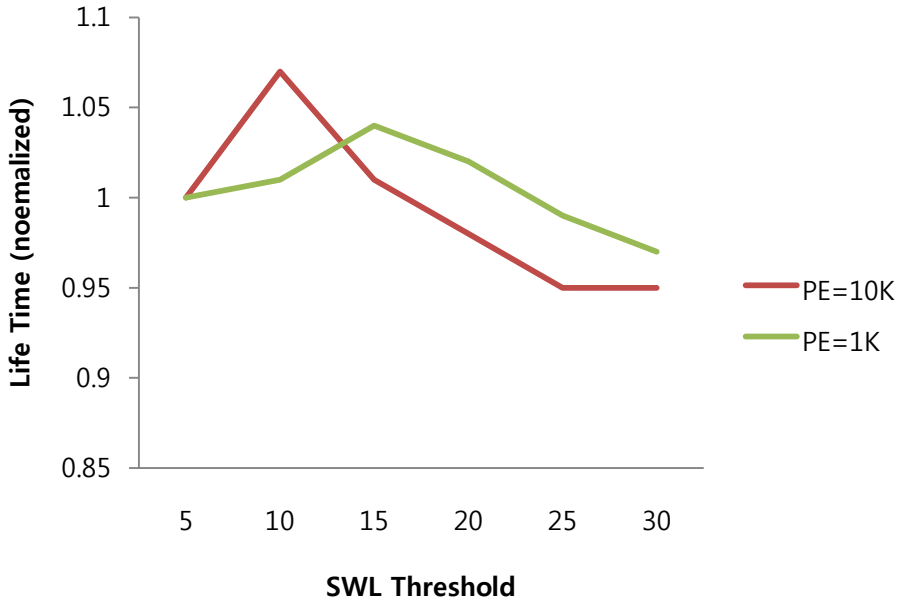
- Static Wear Leveling (SWL)
  - Cold data are copied from young blocks to older so that those young blocks can be erased and written to.
  - This copy actions contribute to wear acceleration.
  - Narrow distribution of erase counts should not trigger static wear leveling.
  - Ultimate purpose of Wear Leveling is not to even out erase counts, but to prolong the life time.





SWL Threshold for TLC

- Increase of total erase count caused by SWL
  - It gets more expensive as PE cycle limit becomes lower.
  - **Variance of erase counts should be tolerated to a larger point.**
- Simulation result

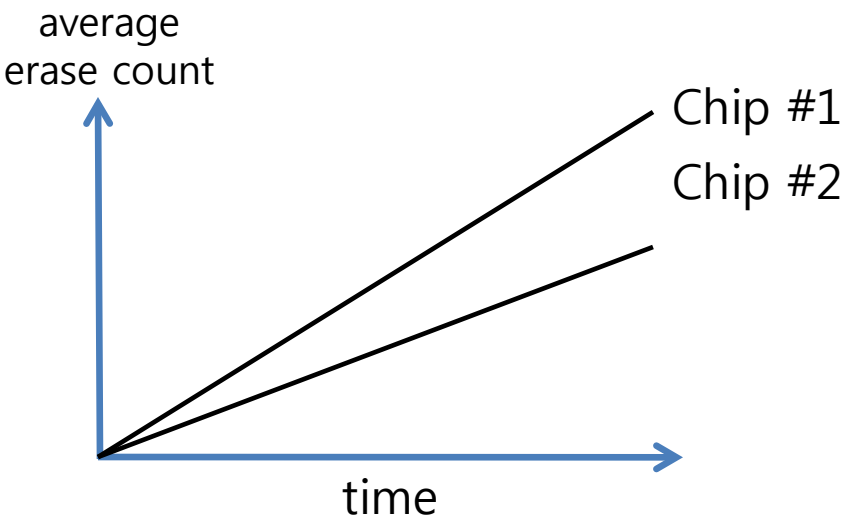


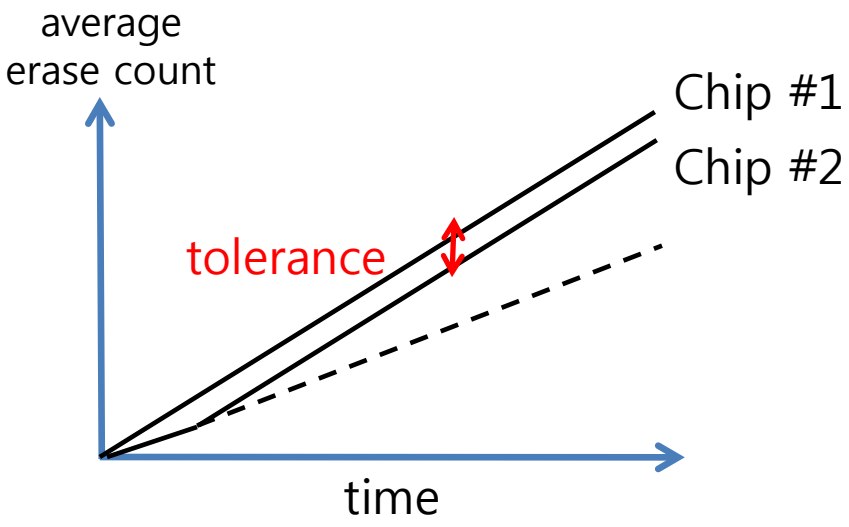
Impact of Over Provisioning

- Over Provision Factor
  - OP = hidden space size / (hidden space size + user space size)
    For example, if a 256GB SSD exposes 238GB space to user, OP = 7%.
  - Wear Leveling can be done more efficiently by increasing the OP.
  - Higher OP alleviates not only Write Amplification, but also Erase Count Variation.
  - However, increasing the OP hurts the price advantage of TLC memory.
  - **Competence of TLC in terms of performance and life time can be achieved by adjusting OP factor.**

Impact of Global Wear Leveling

- Local Wear Leveling
  - Wear Leveling of each NAND Flash chip is independent of each other.
  - Erase count difference between any two chips cannot be removed.
- Global Wear Leveling
  - All chips participate in Wear Leveling decision at the same time.
  - Cold data can be copied from one chip to another.





Impact of Global Wear Leveling (cont'd)

- Life time improvement of GWL over LWL
  - We can easily derive the improvement rate on two chip model.
  - Improvement rate = (2*pe_limit – skew_GWL) / (pe_limit *(1 + skew_LWL))
    skew_LWL = (average erase count of Chip #2) / (average erase count of Chip #1)
    skew_GWL = (average erase count of Chip #1) - (average erase count of Chip #2)
    pe_limit = PE cycle limit of each chip
    Wear acceleration effect is ignored.
- **GWL is less beneficial to 3bit MLC than to 2bit MLC.**
  - Example:
    skew_LWL = 90%
    skew_GWL = 40 (This can be controlled by tolerance constant.)
    when pe_limit = 5000, improvement rate = 1.048 (improved by 4.8%)
    when pe_limit = 500, improvement rate = 1.011 (improved by 1.1%)

Miscellaneous Issues

- Performance of SWL
  - Static Wear Leveling involves copying of multiple pages from a block to another.
  - MSB page shows much longer t_{PROG} than CSB/LSB pages.
  - Three read operations and one Joint Page Program operation can be faster than three copy-back operations.
- Delayed block retirement
  - If erase/program failure occurs due to small number of broken bits, we may still use the block to store cold data, rather than discarding it immediately.
- Bad block count variance
  - Variance of bad block count across multiple chips will be higher for TLC, even with well-controlled erase count distribution.
  - In order to cope with it, we need either inter-chip bad block replacement scheme or globally shared block scheme.