Capacity-approaching Codes for Solid State Storages

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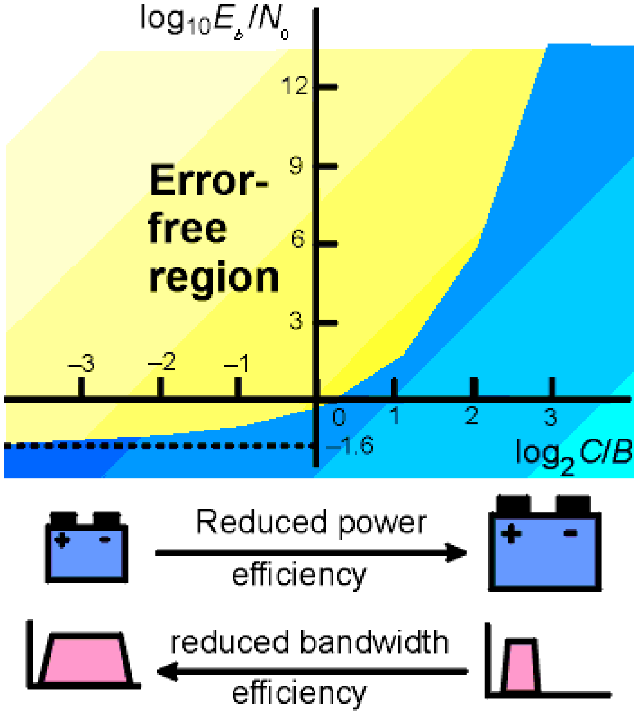
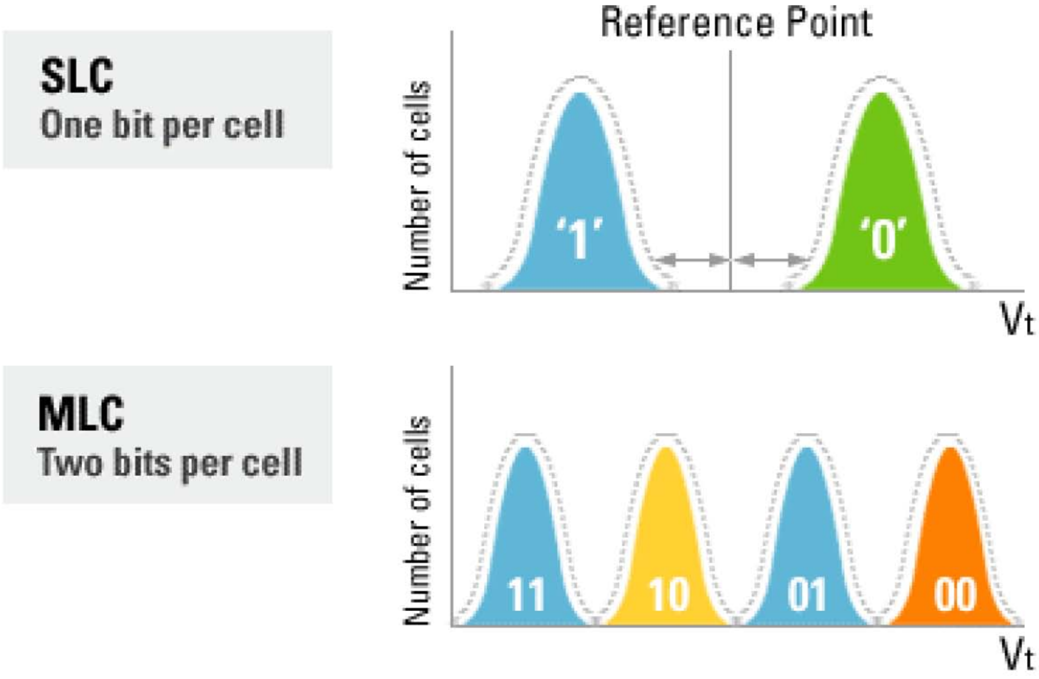
Capacity-Approaching Codes

- Channel Capacity
  - The upper bound on the amount of information that can be reliably transmitted over a communication channel
- Noisy-Channel Coding Theorem
  - The capacity is the limiting information rate that can be achieved with arbitrary small error probability



NAND Flash Memories as Communication Channels

- MLC has a smaller noise-to-signal power ratio (SNR)
- The maximum number of symbol per MLC is predicted by the analysis of channel capacity

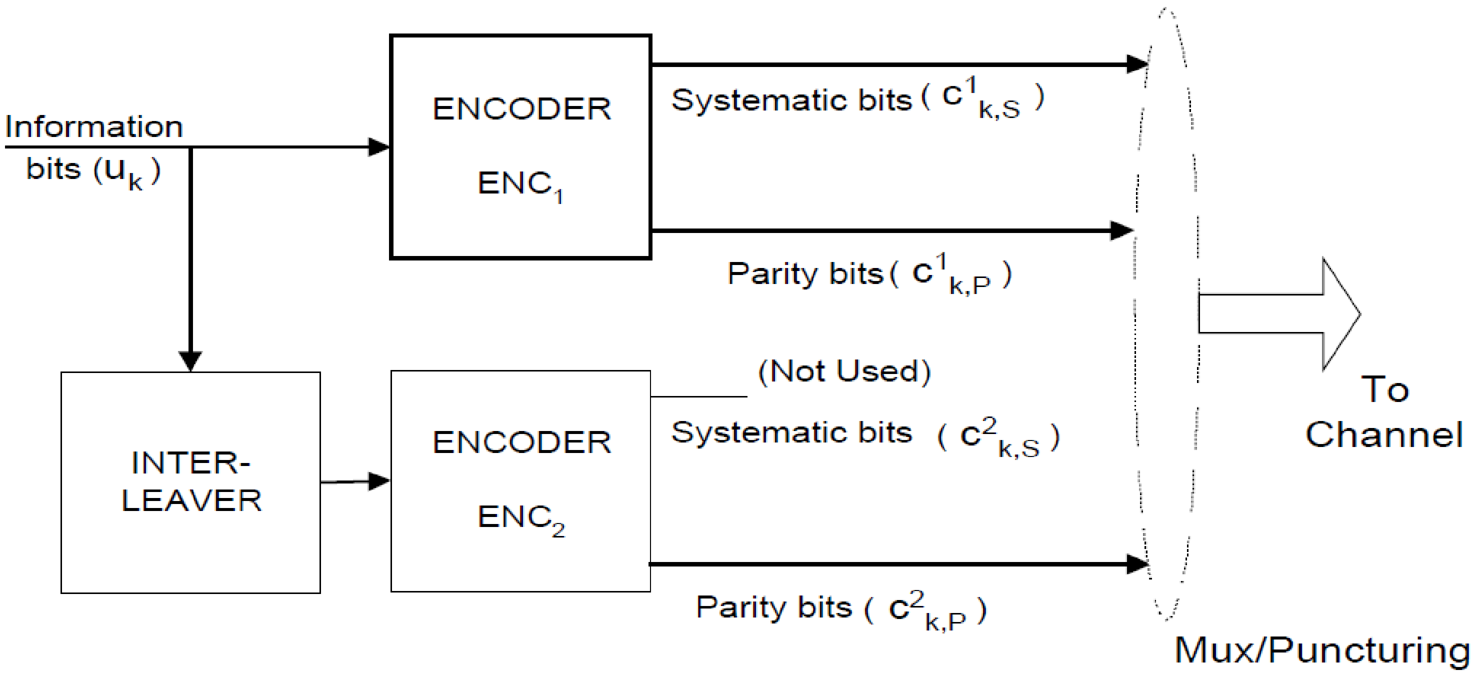


Turbo Codes

- In 1993 (30 years after LDPC codes), C. Berrou, *et. al.* presented their paper, “Near Shannon limit error-correcting coding and decoding: Turbo codes” in ICC93
- The first practical codes approaching Shannon limit
- Parallel (or Serial) Concatenation of Convolutional Codes

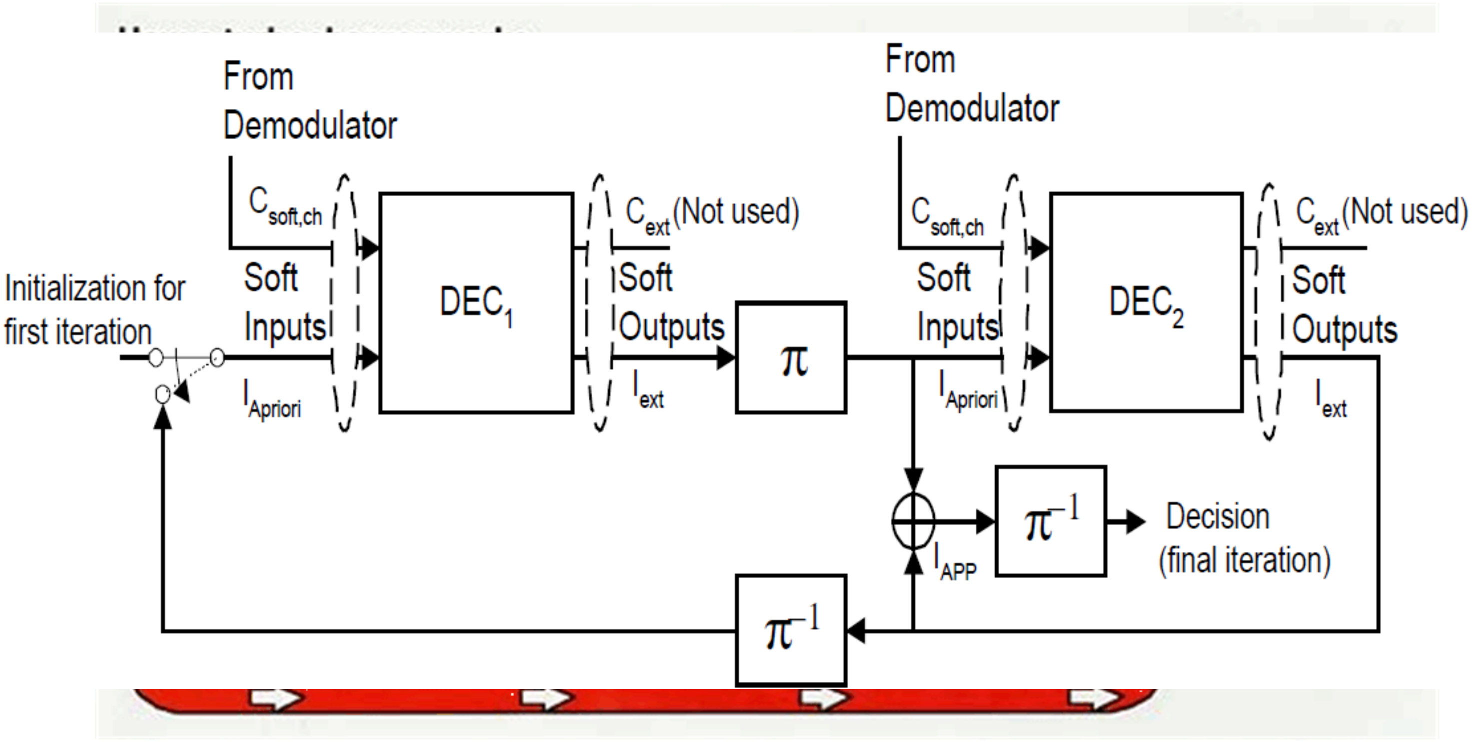
Turbo Codes

- Encoder
  - Parallel Concatenated Convoluational Codes



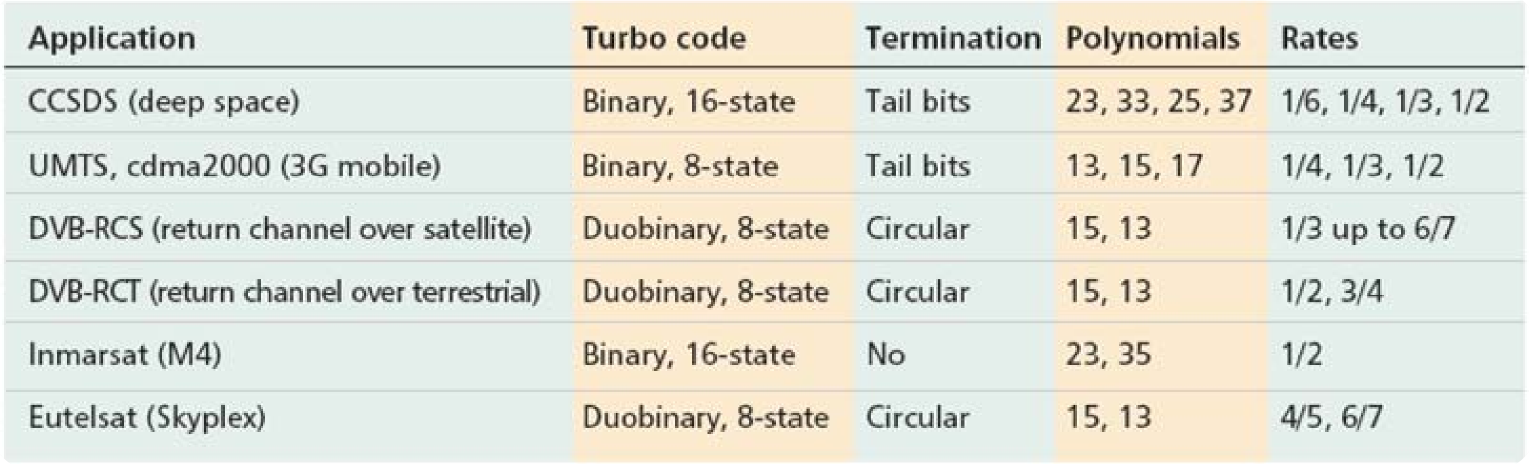
Turbo Codes

- Turbo Decoding
  - Iterative Decoding



Turbo Codes

– Become Dominating Error-Control Codes in Communications



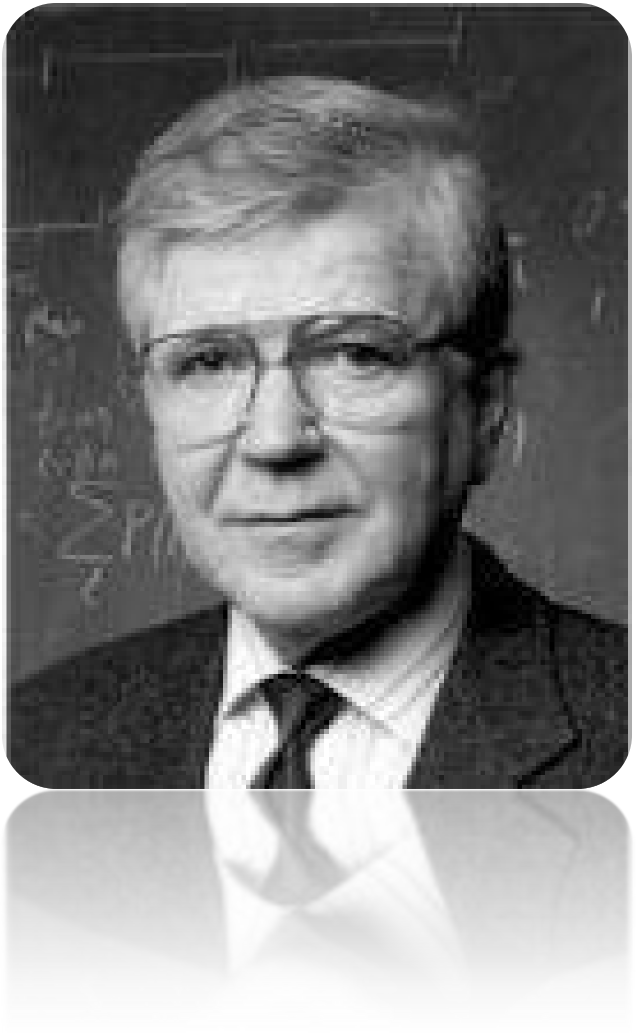
Application	Turbo code	Termination	Polynomials	Rates
CCSDS (deep space)	Binary, 16-state	Tail bits	23, 33, 25, 37	1/6, 1/4, 1/3, 1/2
UMTS, cdma2000 (3G mobile)	Binary, 8-state	Tail bits	13, 15, 17	1/4, 1/3, 1/2
DVB-RCS (return channel over satellite)	Duobinary, 8-state	Circular	15, 13	1/3 up to 6/7
DVB-RCT (return channel over terrestrial)	Duobinary, 8-state	Circular	15, 13	1/2, 3/4
Inmarsat (M4)	Binary, 16-state	No	23, 35	1/2
Eutelsat (Skyplex)	Duobinary, 8-state	Circular	15, 13	4/5, 6/7

Low-Density Parity-Check Codes

- R. G. Gallager (1931 -) proposed "Low-density parity-check codes," IRE trans. Inform. Theory, IT-8, pp. 21-22, Jan. 1962

- D. J. C. Mackay and R. M. Neal rediscovered, "Near Shannon limit performance of low-density parity-check codes," *Electron Lett.*, vol. 32, pp. 1645-1646, Aug. 1996

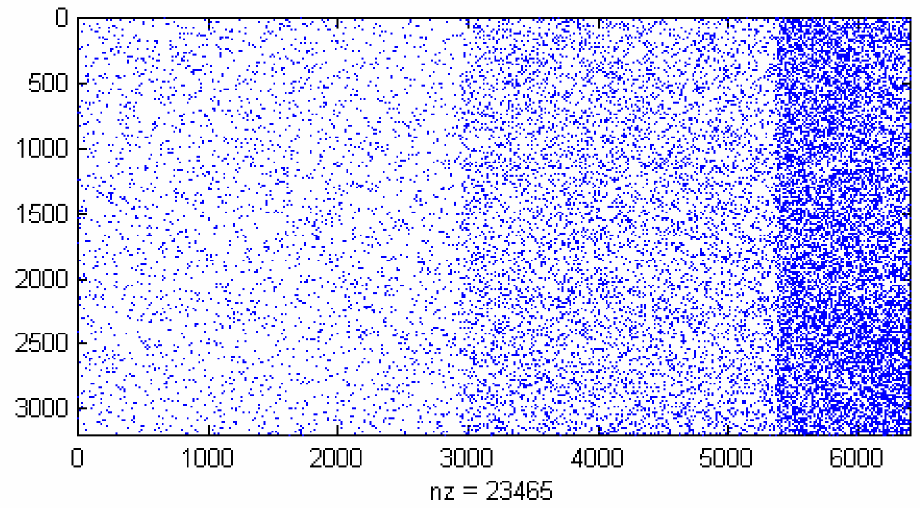
- Belief-propagation algorithm gives us MAP (ML) decoding results, which is working under the message-passing framework



Low-Density Parity-Check Codes

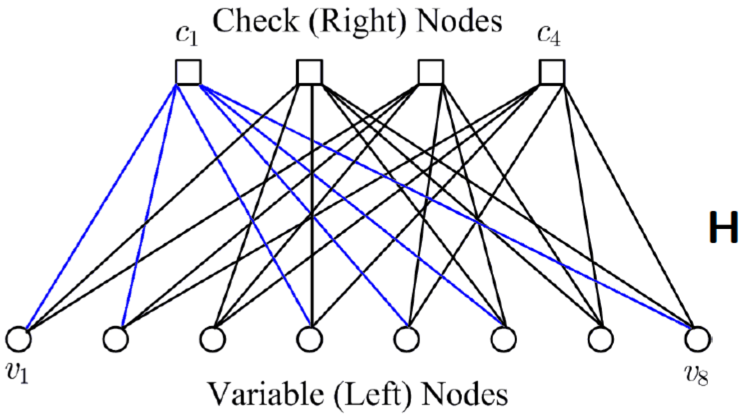
- What Are LDPC Codes?
  - Linear codes
  - Small number of non-zero terms in parity-check matrices

$$\mathbf{0} = \mathbf{c} \cdot \mathbf{H}^T$$



Low-Density Parity-Check Codes

- Representation of an LDPC Code
  - Either Tanner (bipartite) graph or parity-check matrix



Tanner (bipartite) graph

$$\mathbf{H} = \begin{pmatrix} 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \end{pmatrix}$$

Parity-check matrix

Behaviors of Error Control Codes

- Waterfall and Error Floor Regions
  - We are more interested in the *error-floor region*
  - Tradeoff
    - between the performances of waterfall and error floor regions
  - Analysis techniques
    - Waterfall Region
      - Density evaluation, EXIT chart
    - Error Floor Region
      - Minimum distance analysis
      - Trapping set analysis

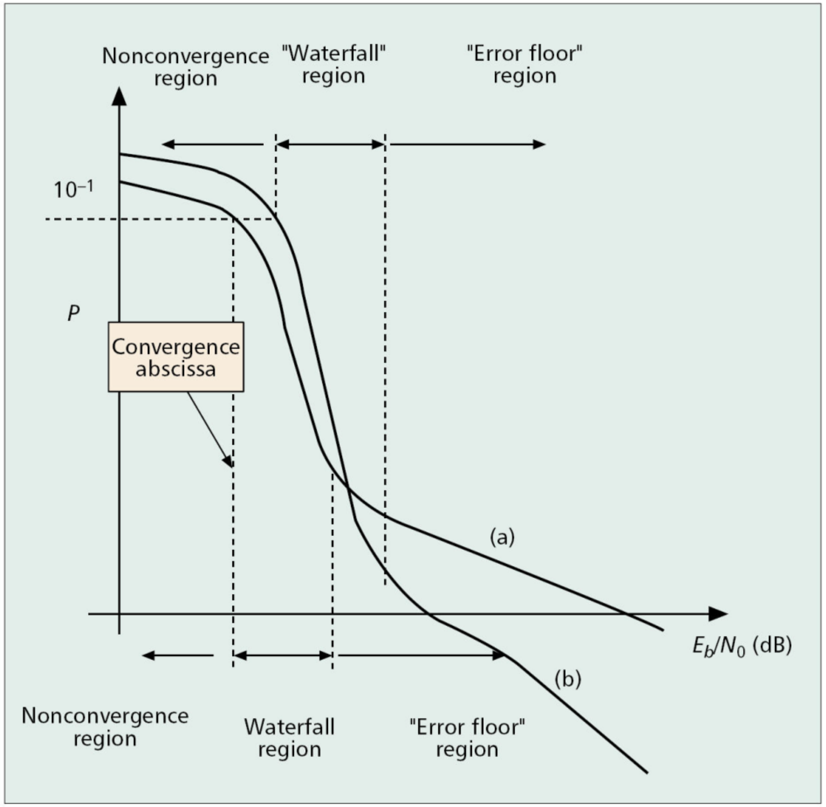
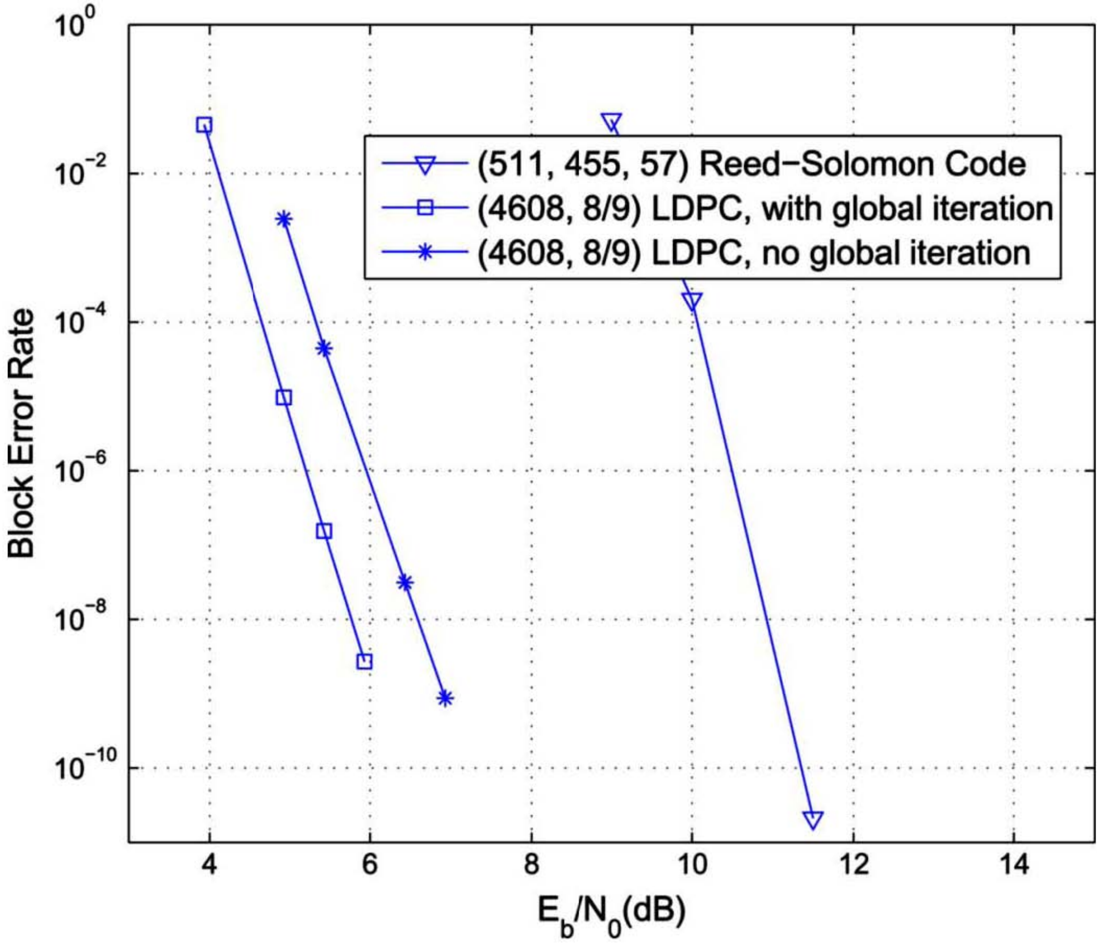
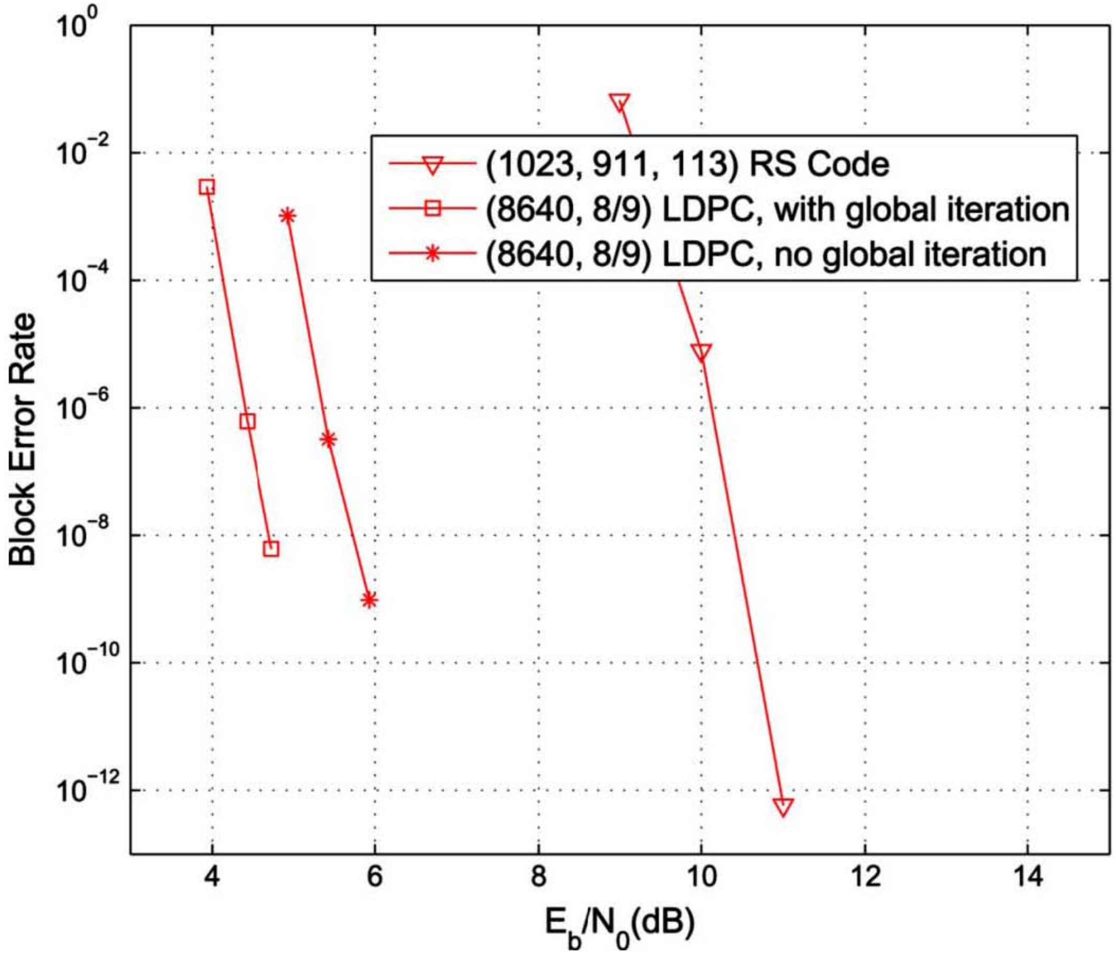


Figure 3. *Qualitative behavior of the error probability vs.* E_b/N_0 *for concatenated codes with interleavers under iterative decoding.*

Successes in Magnetic Storages



Successes in Magnetic Storages

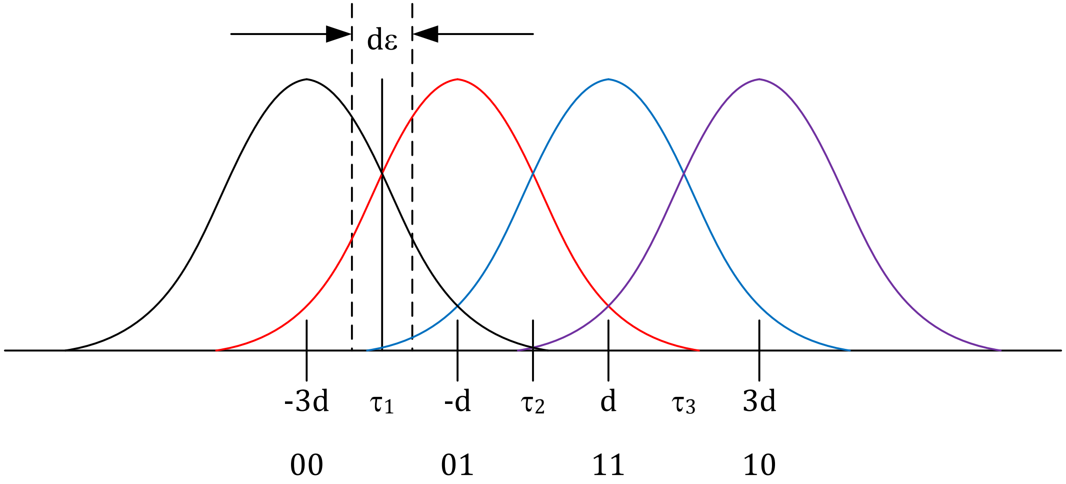


Challenges

- Limited Information from NAND Flash Memory Devices
  - Hard decided bits are available
    - Huge performance loss
      - more than 2dB loss for the convoluational codes
  - Decoding speed and latency
    - High speed belief-propagation decoders need a parallelized structure
      - Bigger die size
    - Iterative algorithms need longer latency

Challenges

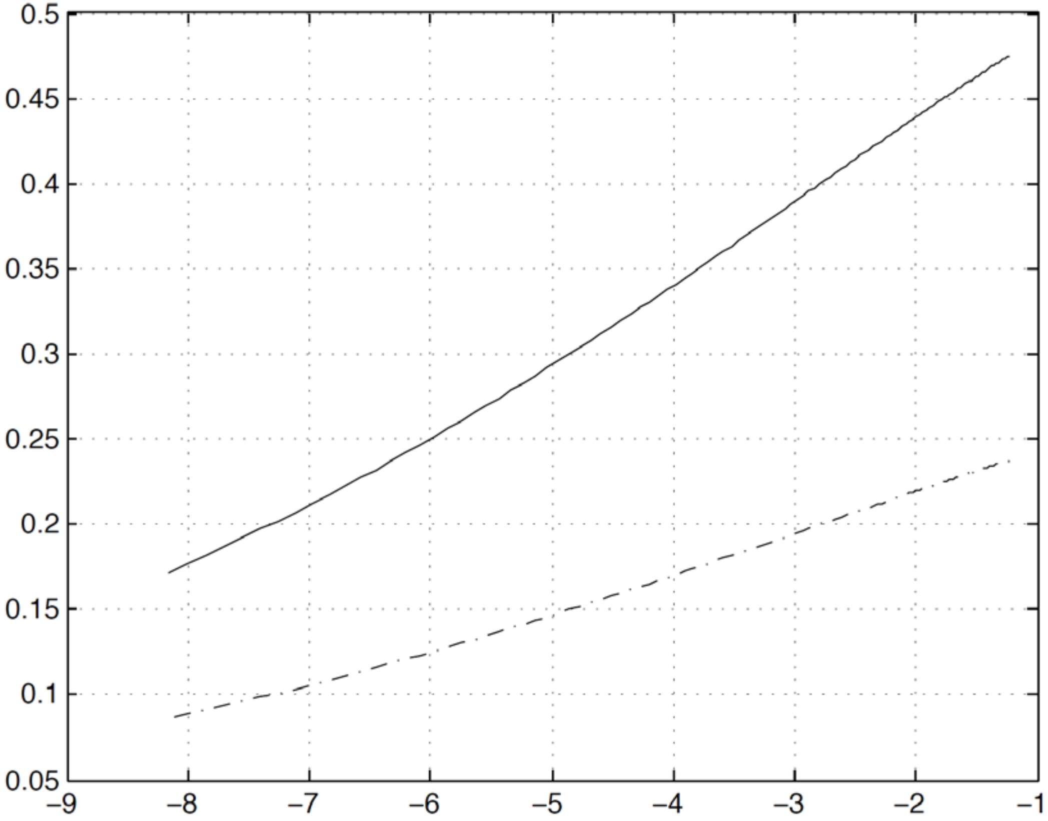
– Performance of Error Control Codes with Side Information, Erasure



$$P_E^B(\mathrm{SNR}) = \frac{1}{\log_2 M} \times \frac{2(M-1)}{M} Q\left(\sqrt{\frac{3}{M^2-1}\mathrm{SNR}}\right)$$

$$\begin{aligned} P_{(E|\mathcal{E})}(\mathrm{SNR}) &= \frac{1}{\log_2 M}\frac{\Pr(\mathrm{E}\cap\mathcal{E})}{\Pr(\mathcal{E})} \\ &= \frac{1}{\log_2 M}\frac{Q\left(\sqrt{\frac{3}{M^2-1}\mathrm{SNR}}\right) - Q\left(\sqrt{\frac{3}{M^2-1}\mathrm{SNR}(1+\epsilon/2)}\right)}{Q\left(\sqrt{\frac{3}{M^2-1}\mathrm{SNR}(1-\epsilon/2)}\right) - Q\left(\sqrt{\frac{3}{M^2-1}\mathrm{SNR}(1+\epsilon/2)}\right)} \end{aligned}$$

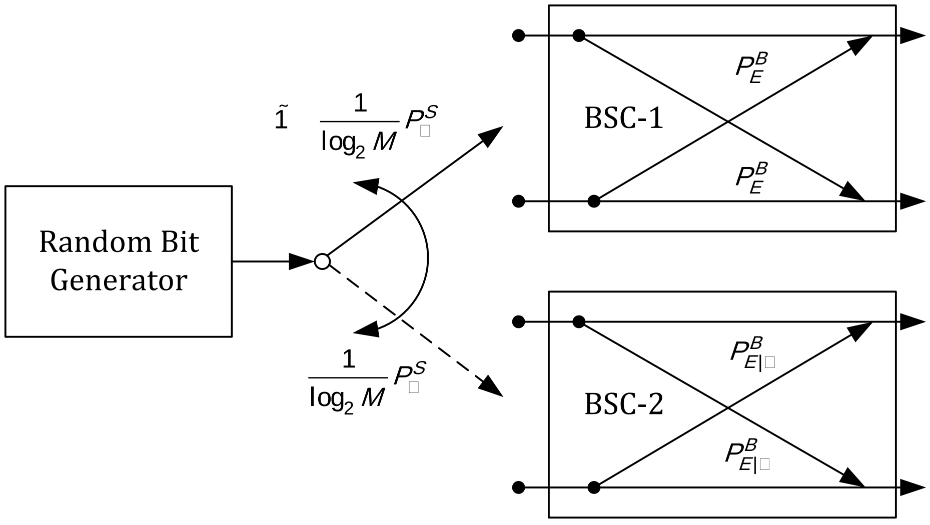
Challenges



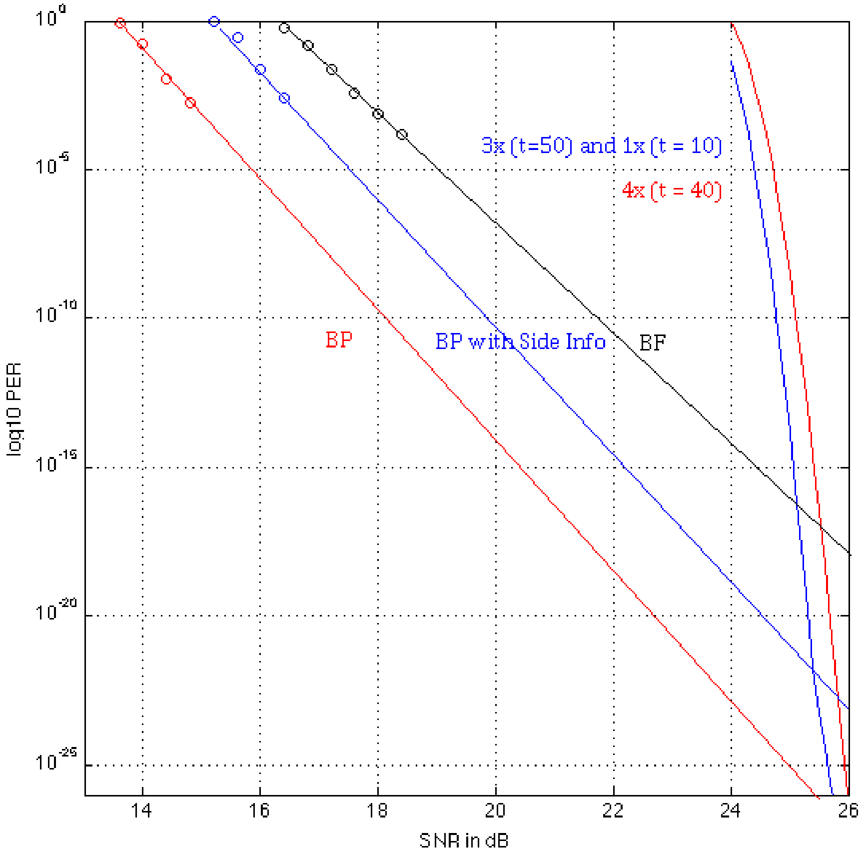
Symbol and bit error rate when the erasure event happens; $\log_{10}(Pe)$ for x axis and then condition probabilities for Y axis

Challenges

- Equivalent Channel Models



Challenges



- The line in blue

  3x(8892,8192,50) BCH Codes and
  1x(8332,8192,10) BCH Code
- The line in red

  4x(8751,8192,40) BCH Codes

Design goal

10^6 pages (4GB) of everyday access
Less than 1% undetectable errors in
1000 days of continuous use

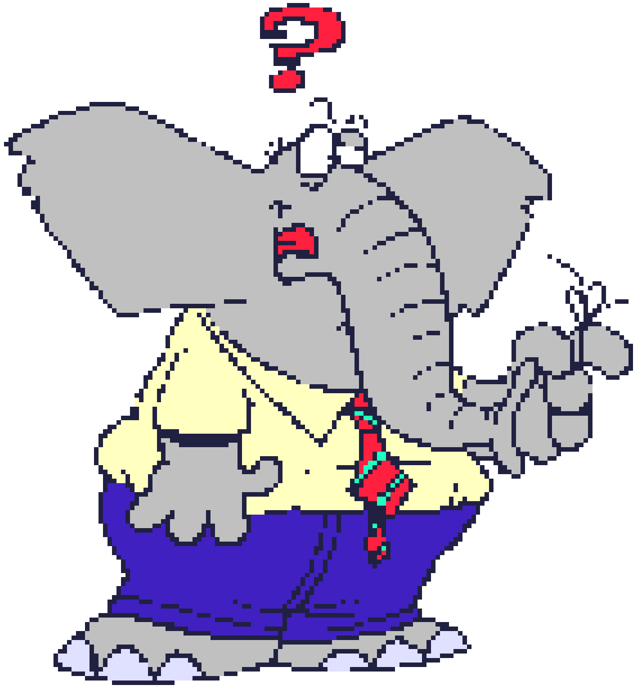
$$
\begin{aligned}
&1-(1-PER)^{10^6\times 1000}\\
&\approx 1-(1-10^9\times PER)\le 0.01\\
&\rightarrow PER\le 10^{-11}
\end{aligned}
$$

Summary

- Introduction to Capacity-approaching Codes
- Discussions about Challenges in Solid State Drives

- Active Collaborations with People in Other Fields Are in Need
  - Especially with Device Engineers

Q&A



Challenges

- Decoding Speed

Processing Modules (PM)	FFs	Memory	Ratio: 1/2	Ratio: 2/3A	Ratio: 2/3B	Ratio: 3/4A	Ratio: 3/4B	Ratio: 5/6
1	2.8K	160Kbits	0.65 5.2 Mbit/s 2.6 Mbit/s	0.74 5.92 Mbit/s 3.94 Mbit/s	0.74 5.92 Mbit/s 3.94 Mbit/s	0.79 6.32 Mbit/s 4.74 Mbit/s	0.79 6.32Mbit/s 4.74 Mbit/s	0.84 6.72 Mbit/s 5.60 Mbit/s
6	14K	160Kbits	3.71 29.68 Mbit/s 14.84 Mbit/s	3.71 29.68 Mbit/s 19.78 Mbit/s	3.71 29.68 Mbit/s 19.78 Mbit/s	4.39 35.12 Mbit/s 26.34 Mbit/s	4.39 35.12 Mbit/s 26.34 Mbit/s	4.39 35.12 Mbit/s 29.26 Mbit/s
8	20K	300Kbits	4.88 39 Mbit/s 19.5 Mbit/s	5.66 45.28 Mbit/s 30.18 Mbit/s	5.66 45.28 Mbit/s 30.18 Mbit/s	5.66 45.28 Mbit/s 30.18 Mbit/s	5.66 45.28 Mbit/s 30.18 Mbit/s	6.42 51.36 Mbit/s 42.8 Mbit/s