Consideration for Determining Page/Block Size in NAND Flash

Hynix Semiconductor Inc.

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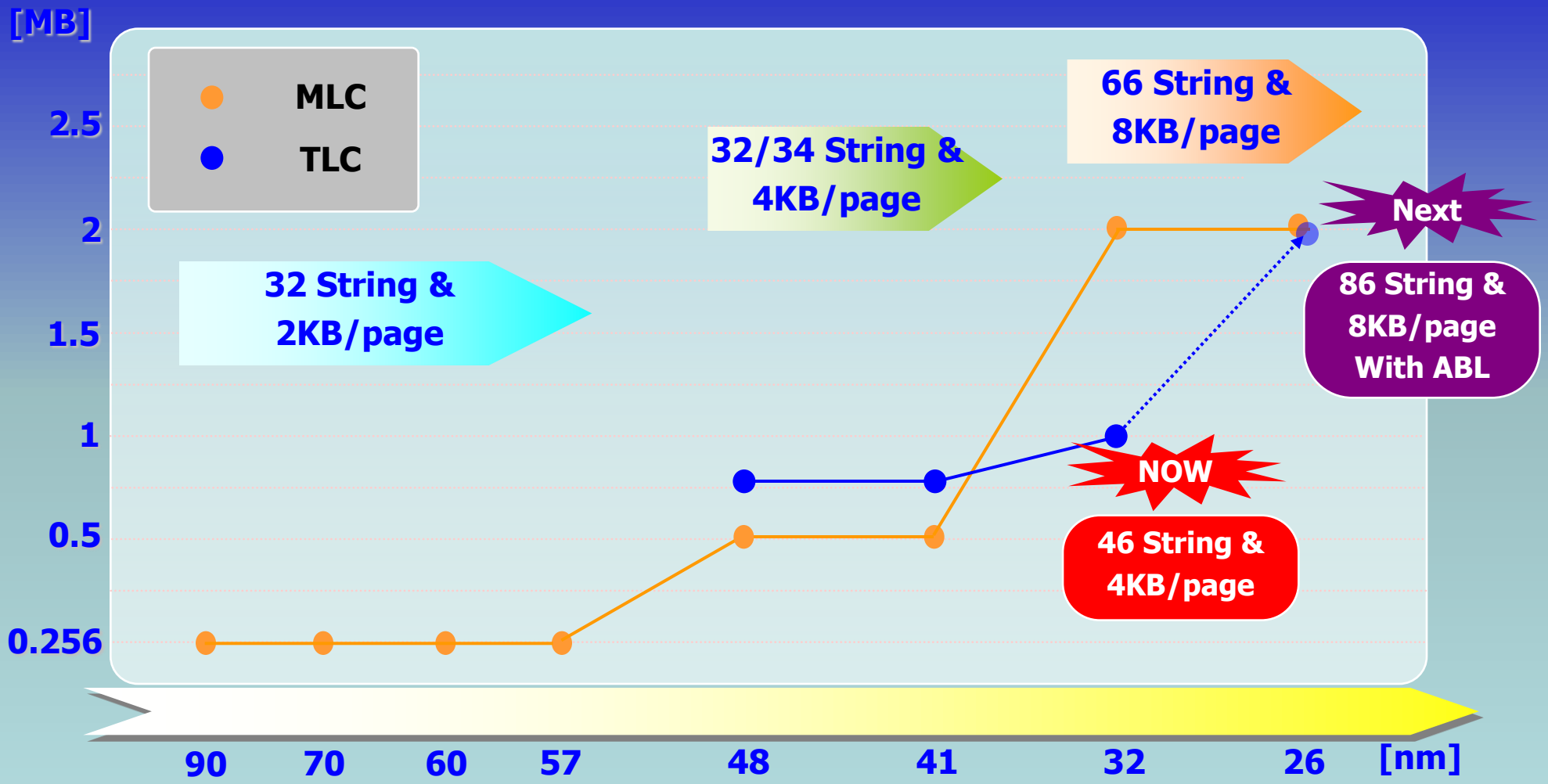
Hynix NAND Block Size Trend



Factor of the Increasing Page/Block Size

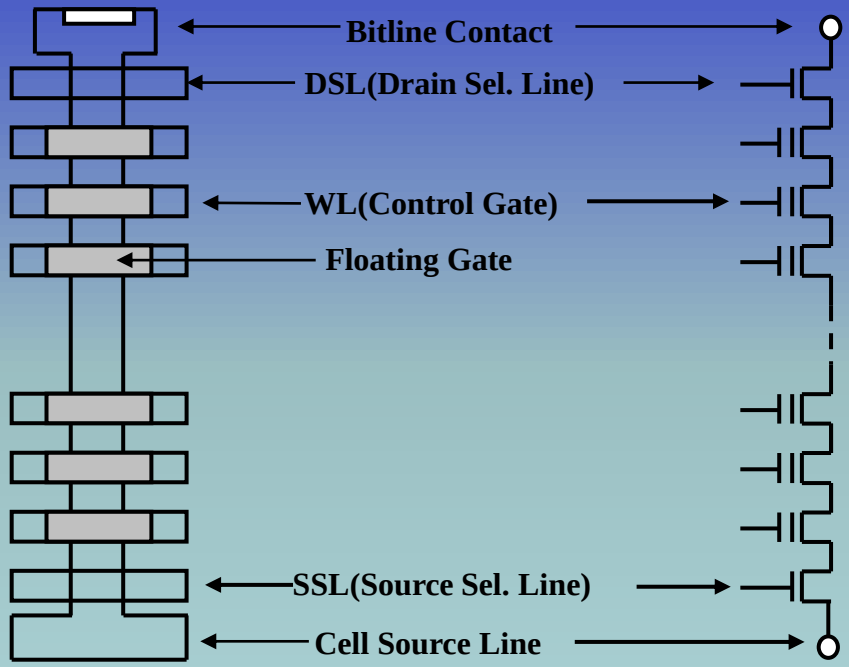
Block Size = page num * page size
= (bit /cell) * string num * E/O * page size

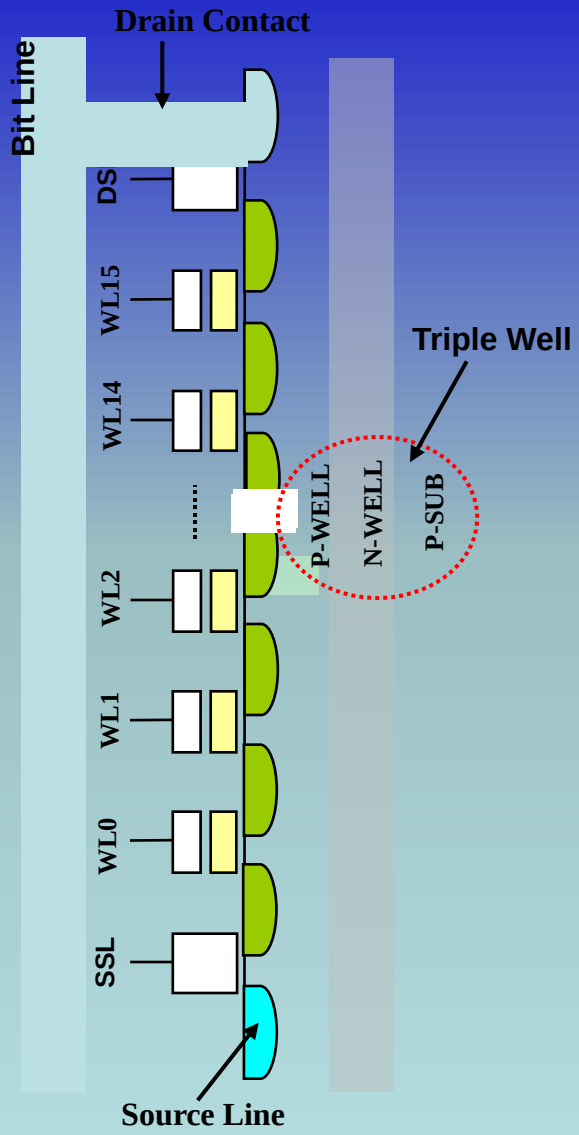
Item	Trend	Characteristics
Bit / cell	SLC → MLC → TLC	+) bit growth ↑ −) tPROG/tR/Reliability ↓
String	32 string → 64 string	+) bit growth ↑ −) disturbance ↑
Page size	2KB → 4KB → 8KB	+) performance ↑ −) chip size ↑
Bit Line	EOBL → ABL	+) block size ↓ −)

Architecture & Specification

- **What's a cell string?**

; Cell Operation Unit of Read/Program

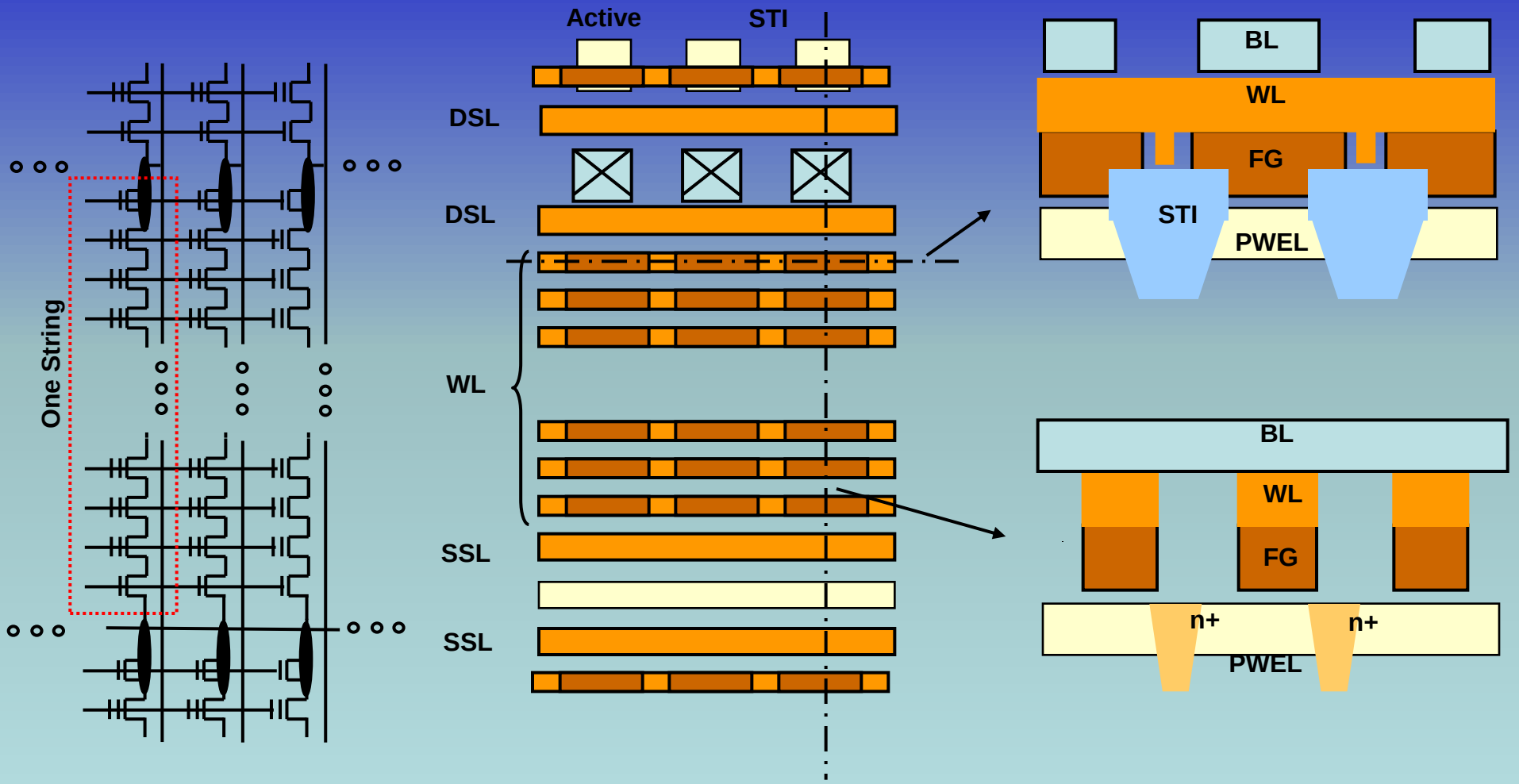




Tech.	0.12um	0.09um	0.07um
String	16	32	32
Density	512M, 1G	512M,1G,2G	1G,2G,4G

Architecture & Specification

- **NAND Cell Array**



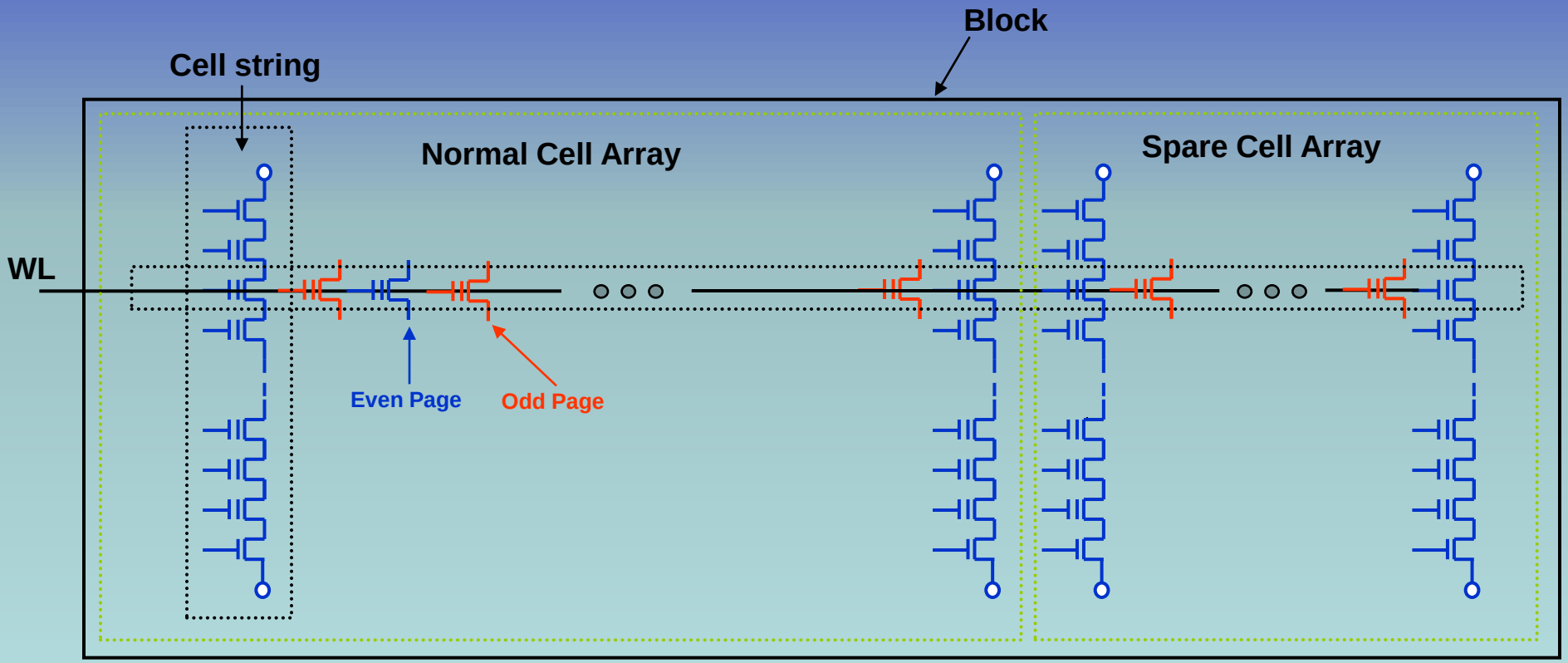
Architecture & Specification

- **Page & Block**

  -Cell Array = Normal cell + Spare cell

  -What's a cell string, a page and a block ?

  -One word line = Even page + Odd page



Thank You