Flash Memory: Key Signal Processing Issues

Jaekyun Moon

EE Dept KAIST

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HDD vs SSD: Price Trend



SSD prices were assumed to fall by about <u>60% annually</u>.





연도별 HDD와 SSD의 GB당 가격 비교 (출처: iSuppli)



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Home Storage Server



Home Storage Server



1TB NAS Server, 480/12 Mbps \$138.00

Price: \$0.14/GB



Flash Memory in IPad

\$499 for 16G iPad versus \$699 for 64G iPad





Sustaining Storage Density Growth...



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Outline

- How many raw errors can we realistically correct using advanced SSP?
 - LDPC code versus BCH
- Essential Ingredients
 - Channel characterization (J. Moon)
 - Capacity-achieving coding (J.S. Ha)



MLC NAND Flash Architecture

A 2-plane, 4K-page MLC architecture. The 4K page has 4,096 bytes of data and 218 bytes of spare area.



A 16Gb MLC NAND Flash Example





SSP Signal Flow





BCH Code Performance: Raw BER vs Corrected WER



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LDPC Code Performance



LDPC can handle 10^(-1.913)*9830=120 error bits on average per 9830 bits (Probably ideal and optimistic).



Real LDPC Error performance (10G Ethernet) – no visible error floor (gives us hope!)



Source: G. Ungerboeck, 2010

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Essential Ingredients in Advanced SSP

- Accurate channel characterization
- Soft information generation and processing



Channel Modeling: Signal–Level Characterization of Cell Correlation (Disturb)



Channel Modeling: Cell Correlation







Feed the system with known data \mathbf{x} . Observe \mathbf{r} .

Characterize the system enough, so for new data **x**' we would know what **r**' is.



Channel Identification Problem



Feed the system with known data **x**.

Adjust f() until **e** is minimized (a sequential update algorithm is used).

Once **e** stabilizes, f() should resemble the system closely.

We in essence are fitting the unknown box with a partially unknown function (a certain structure is imposed)



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Characterized Channel







Example of f(): Linear FIR Filter



Popular model for one dimensional inter-symbol interference



A general f(): RAM



f() is a RAM and its contents get updated in the direction to minimize **e**. The write values of a cell and its affecting cells act as the pointer (address) to a particular location in the RAM. The RAM content is the read value of the victim cell.

After feeding the system and the model with a long data \mathbf{x} , all locations of the RAM will have been updated and stabilized.



RAM Update Process: An Example of "Local" Pattern





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RAM Update Process





A general f(): RAM



Assumption: correlation among a cell and its affecting cells is positionshift-invariant.

If x_k is affected by x_{k-1} and x_{k+1} in a certain way, then x_{k+1} will be affected by x_k and x_{k+2} in the same way.



Some of the discussion points …

- Are there such thing as the rough "local" pattern and can device people figure this out, if so?
 - Exact function can be obtained via statistical identification as described
- Feasibility of extracting soft information

