Enabling TB-Class and GB/s-Performance SSDs with HLNAND™

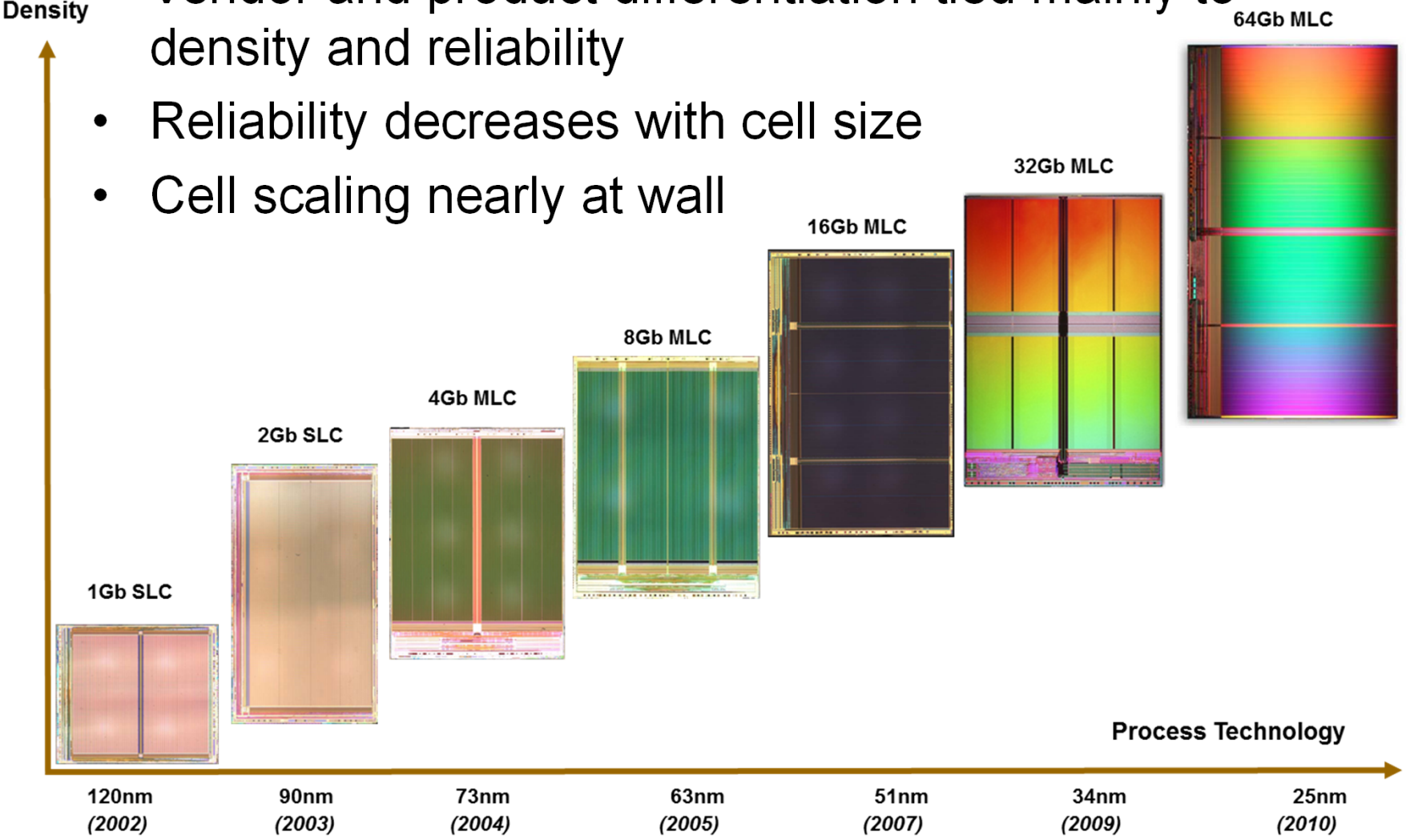
November 2011

Agenda

- Introduction
- HyperLink NAND (HLNAND) Flash Technology
- Signal Integrity
- Summary

NAND Flash History

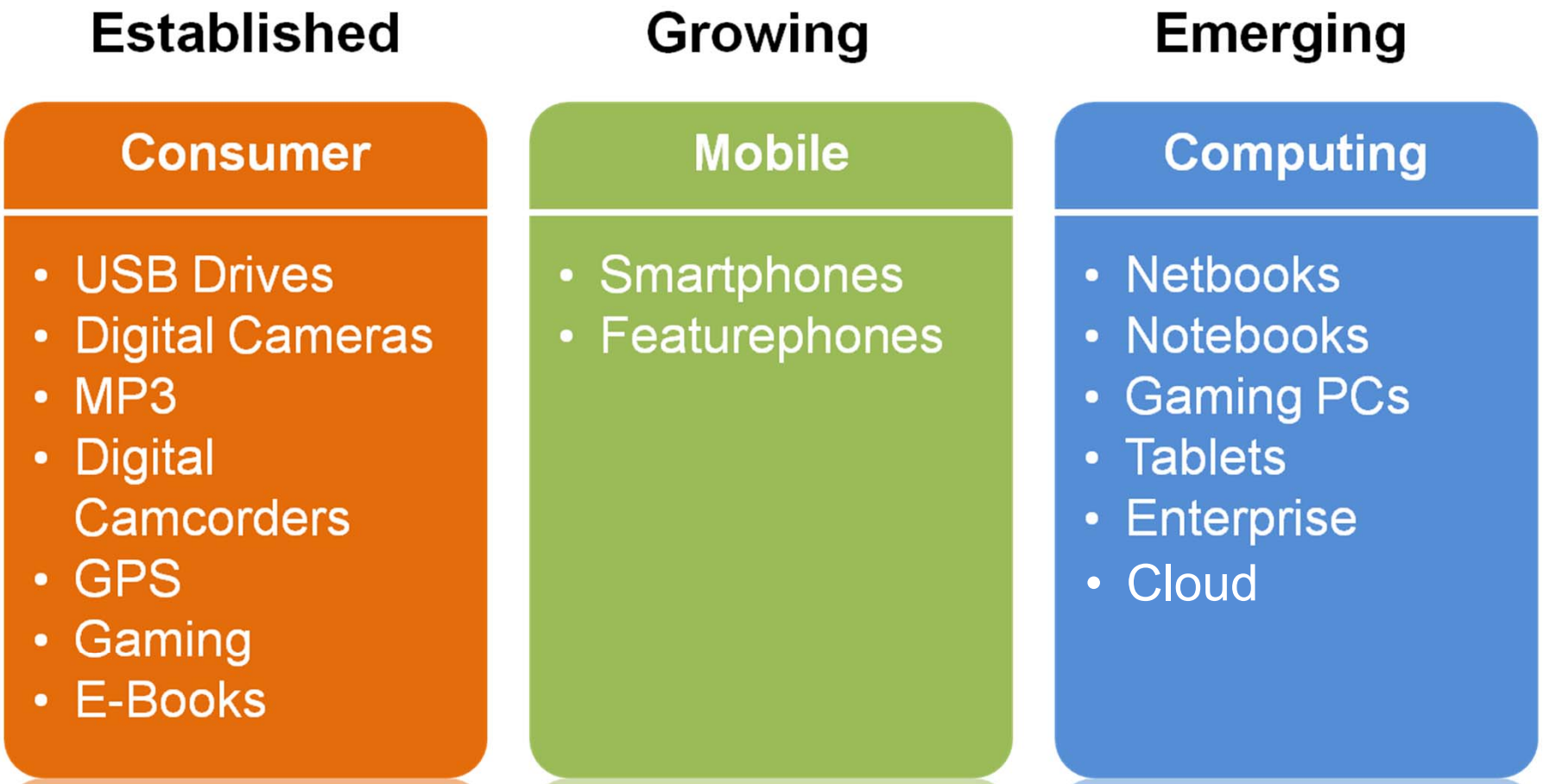
- Vendor and product differentiation tied mainly to density and reliability
- Reliability decreases with cell size
- Cell scaling nearly at wall



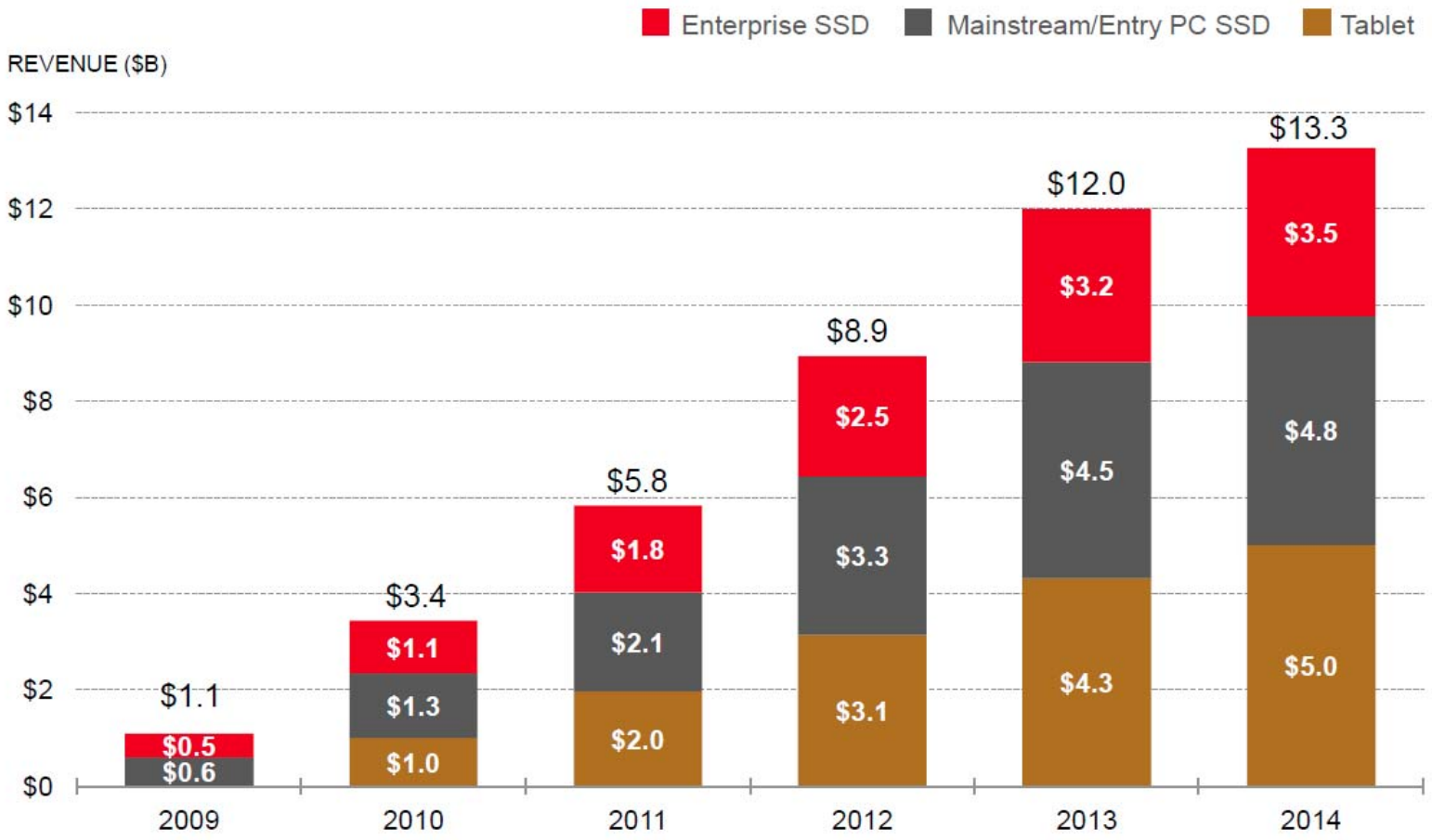
Nearly at Scaling Wall, What's Next?

- How will Flash producers make a compelling story at the wall?
- Reliability will still play a differentiating role
- Feature enrichment and performance improvements will also help distinguish products and serve product niches

Flash Market Landscape



Flash-based Emerging Market



Source: Gartner November, 2010; Semiconductor Forecast Worldwide—Forecast Database [SEQS-WW-DB-DATA]
Numbers are preliminary and subject to change

Source: SanDisk Feb 2011

Consumer SSD Market

200+ SSD vendors, but little differentiation

Enterprise-Grade Storage SSDs

Critical Factors:

- Reliability
- Performance/Power
  (High IOPS & Throughput)
- Scalability

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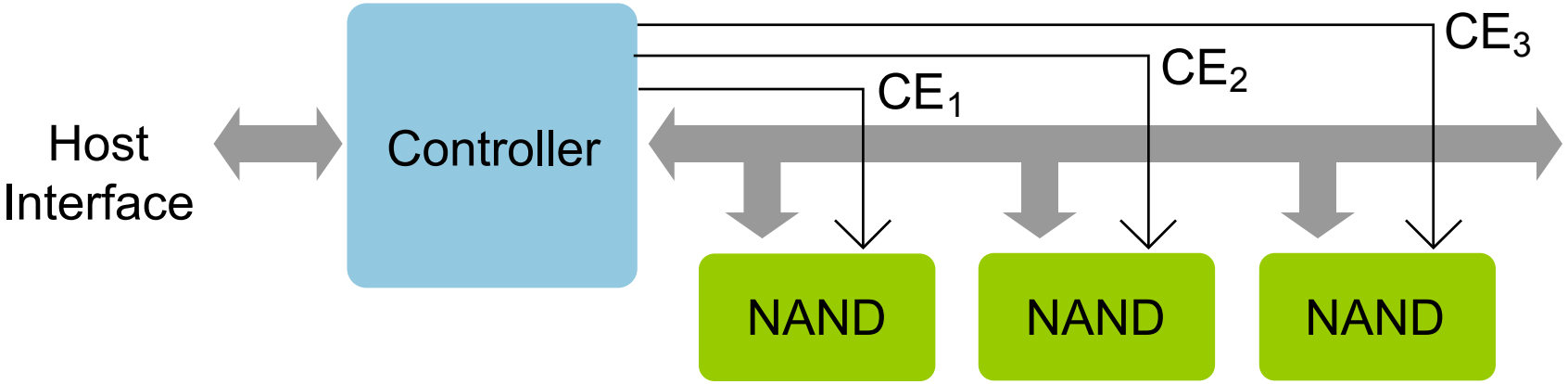
- Signal Integrity
- Summary

Conventional NAND Flash Interface

- 8 bit, bidirectional, multi-drop bus
- Asynchronous LVTTL signaling up to 40Mb/s/pin
- Speed degradation with more than 4 devices on bus
- Chip Enable (CE) signal required for each device
- Power hungry 3.3V I/O or 1.8V I/O
- Recently DDR NAND (ONFI, Toggle) introduced



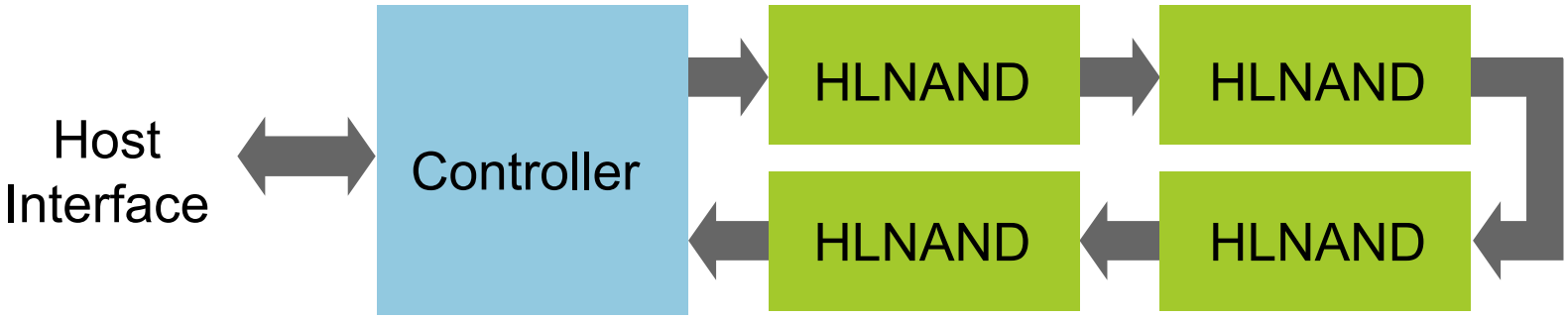
Performance and Scalability
(Multi-drop Bus)

- Adding more channels:
  - System design complexity
  - Poor Signal Integrity (SI)
  - Higher power consumption
  - ECC/IO overhead per channel
  - Complex PCB design requiring 7-10 layers

- Adding more devices per channel:
  - Compromise between performance and # of devices

HLNAND Topology

- Daisy-chain, point-to-point connection – ring topology
- Cleaner signaling than multi-drop bus
- High speed and no-roll-off with increasing load



Performance and Scalability
(HLNAND Ring Topology)

- Higher performance 800MB/s and beyond (compared to 200MB/s & 400MB/s for conventional architecture)
- Virtually unlimited number of devices can be cascaded (higher number of ways per channel)
- Minimizing the number of channels per system

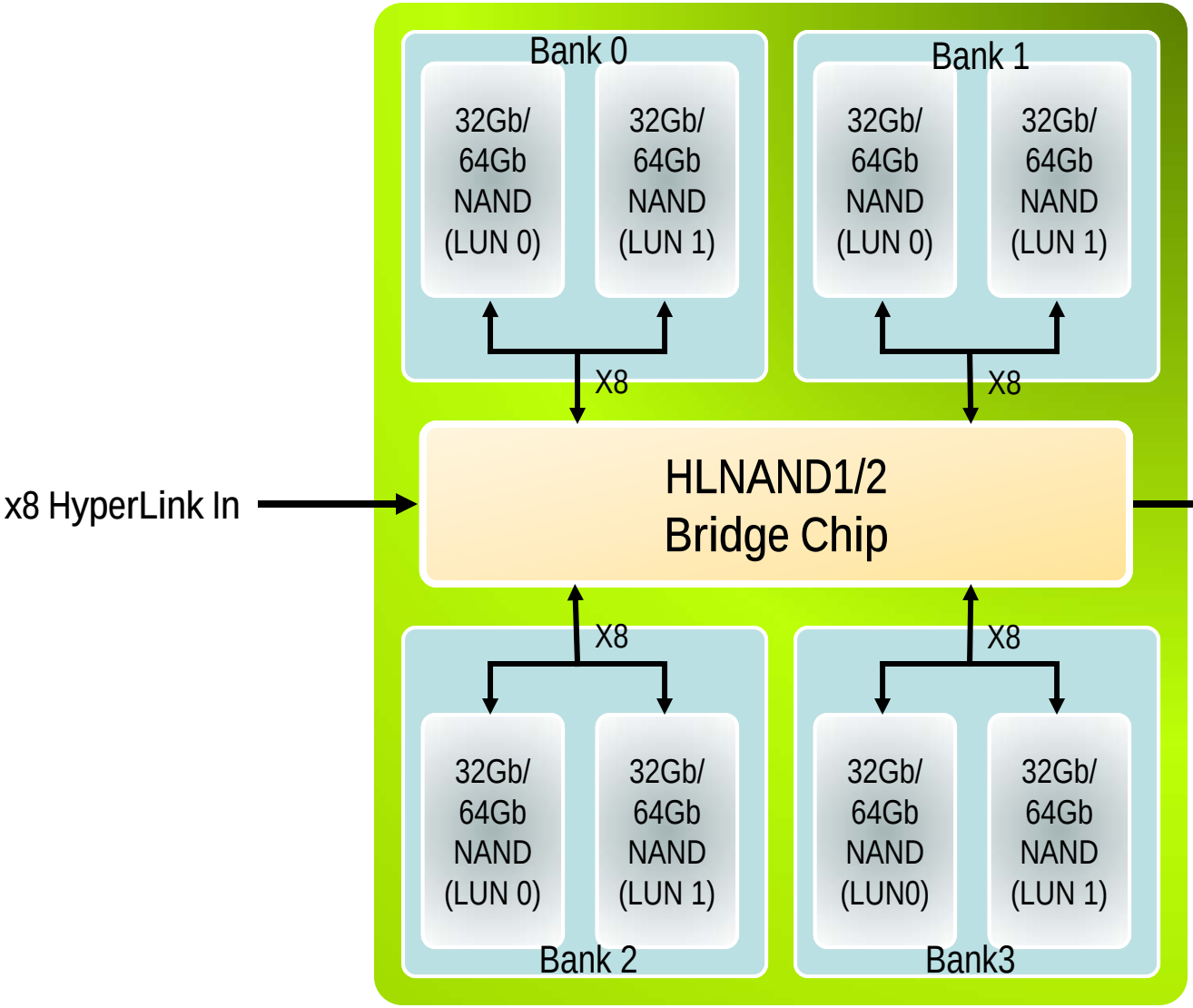
Performance and Scalability
(HLNAND Ring Topology)

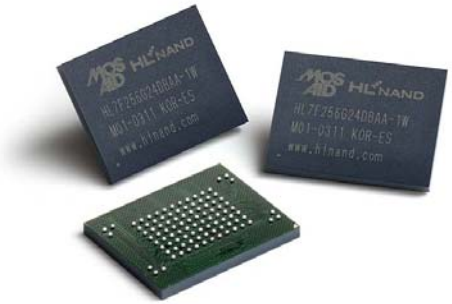
- Superior signal integrity (SI)
- No ODT required
- Statistically 50% lower power consumption per channel due to power-saving feature
- Scalable without diminishing performance for Tera Byte-Class & GB/s-Performance SSDs

HLNAND Parts

	HLNAND 1.0 (DDR266)	HLNAND 2.0 (DDR533/667/800)
E/S Sample	Available	Available
HLNAND Interface Chip	TSMC 180nm	TSMC 90nm
NAND Core	32nm/2xnm Async. or DDR-type NAND	32nm/2xnm Async. or DDR-type NAND
MCP Memory Capacity	128Gb ~ 1Tb (4 ~ 16 die stacked)	128Gb ~ 1Tb (4 ~ 16 die stacked)
I/O Data Rate	266 MB/s	533/667/800 MB/s
Package	14mm x 18mm 100-ball BGA	14mm x 18mm 100-ball BGA

HL & HL2 MCP Architecture

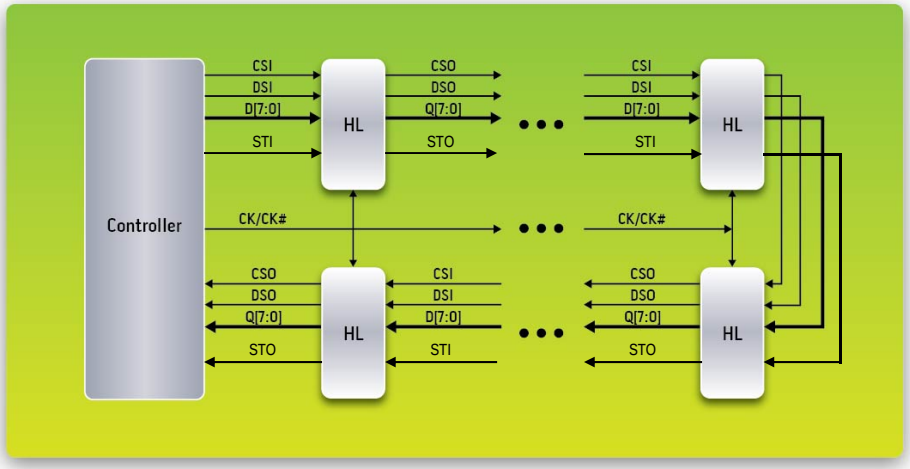




- Four-bank architecture
- Fully independent LUN (Logical Unit) operation

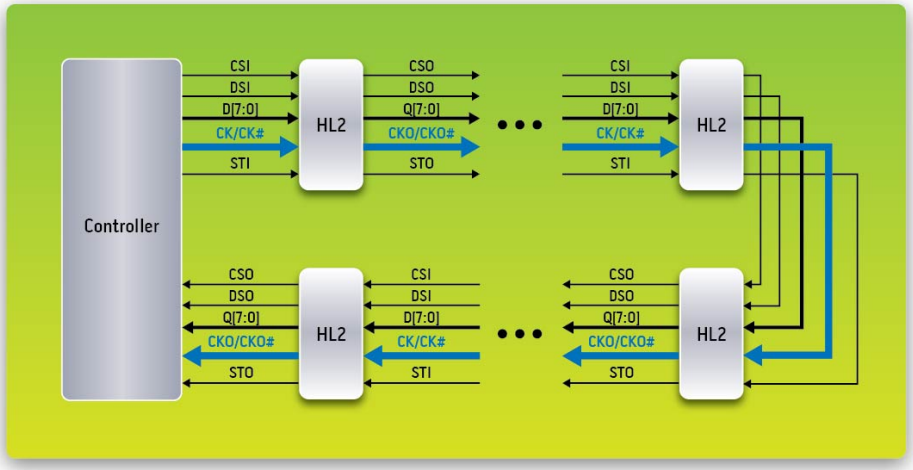
HLNAND vs. HLNAND2

HLNAND (HL1)



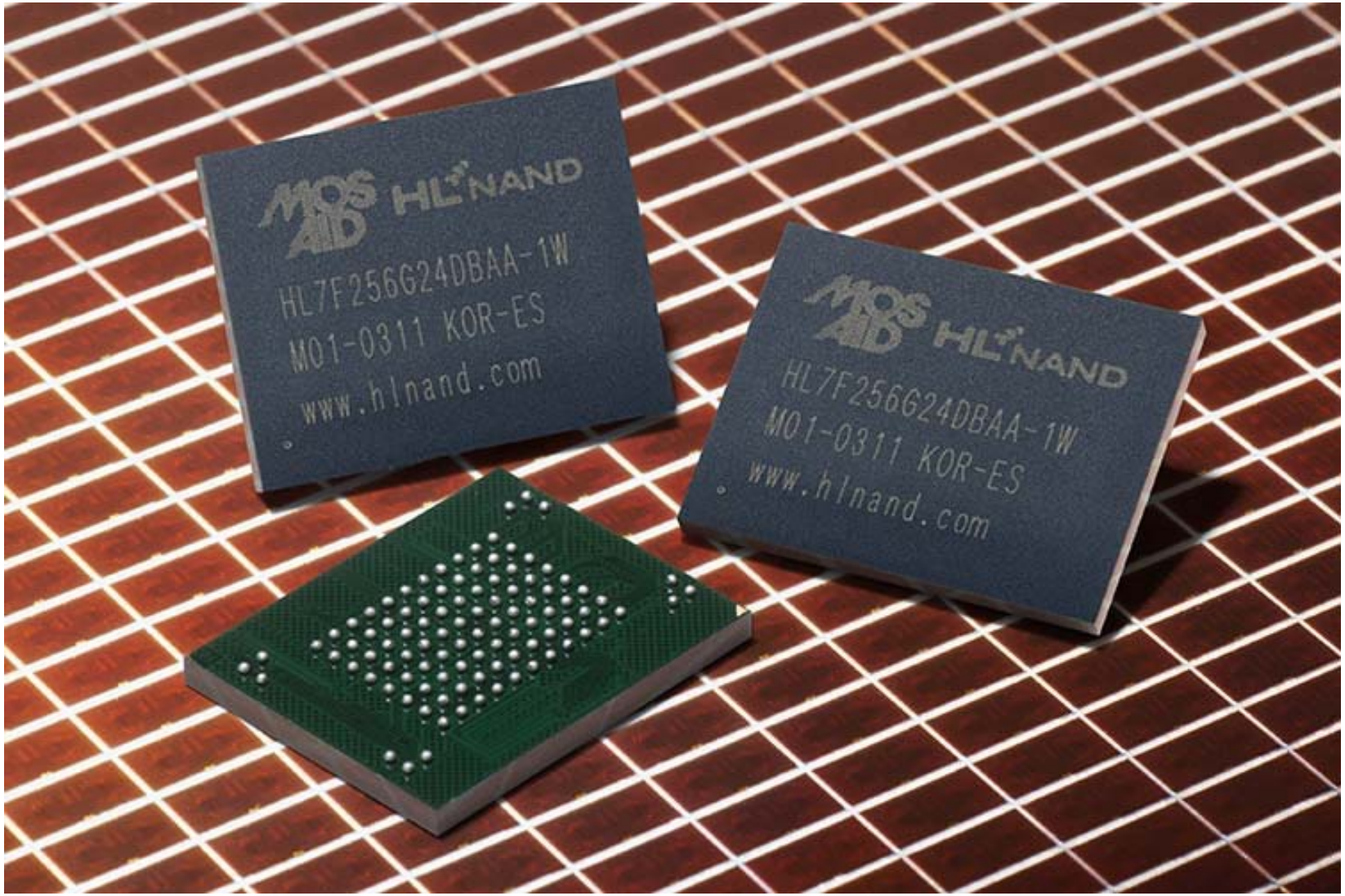
- Up to DDR-266
- Parallel distributed clock
- 1.8V LVCMOS

HLNAND2 (HL2)



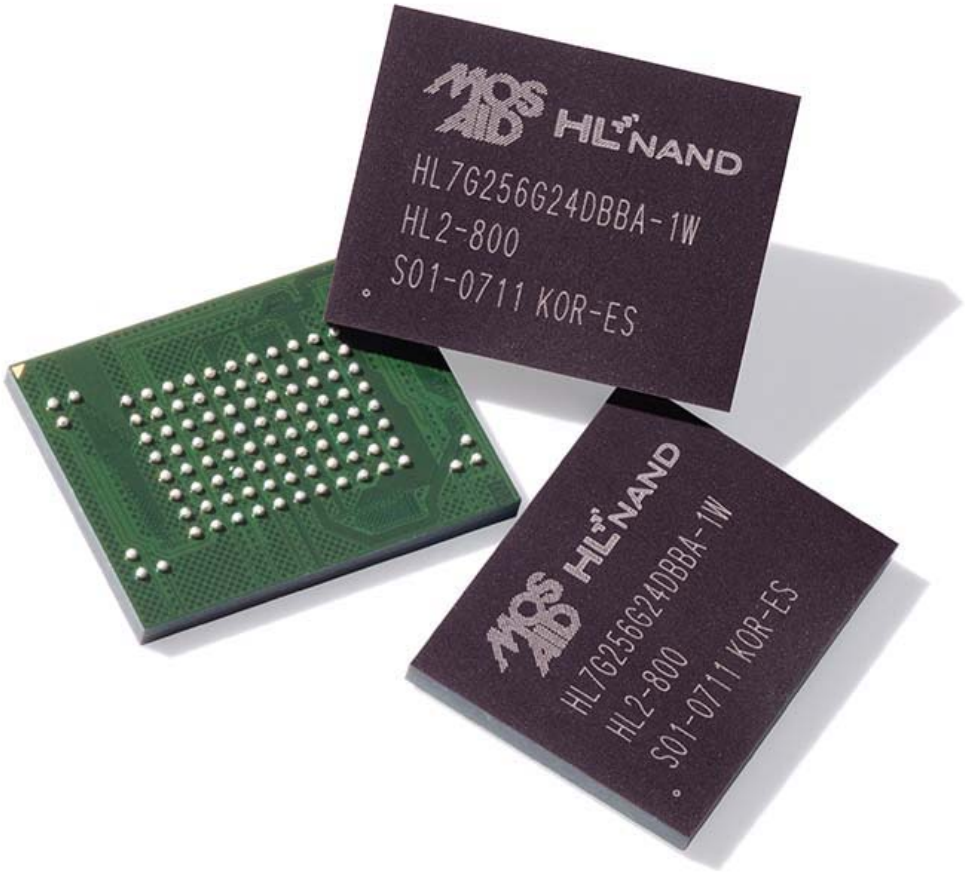
- DDR-533/DDR-667/DDR-800
- Source-synchronous differential clock
- JEDEC 1.2V HSUL_12

256Gb HLNAND E/S in 2011

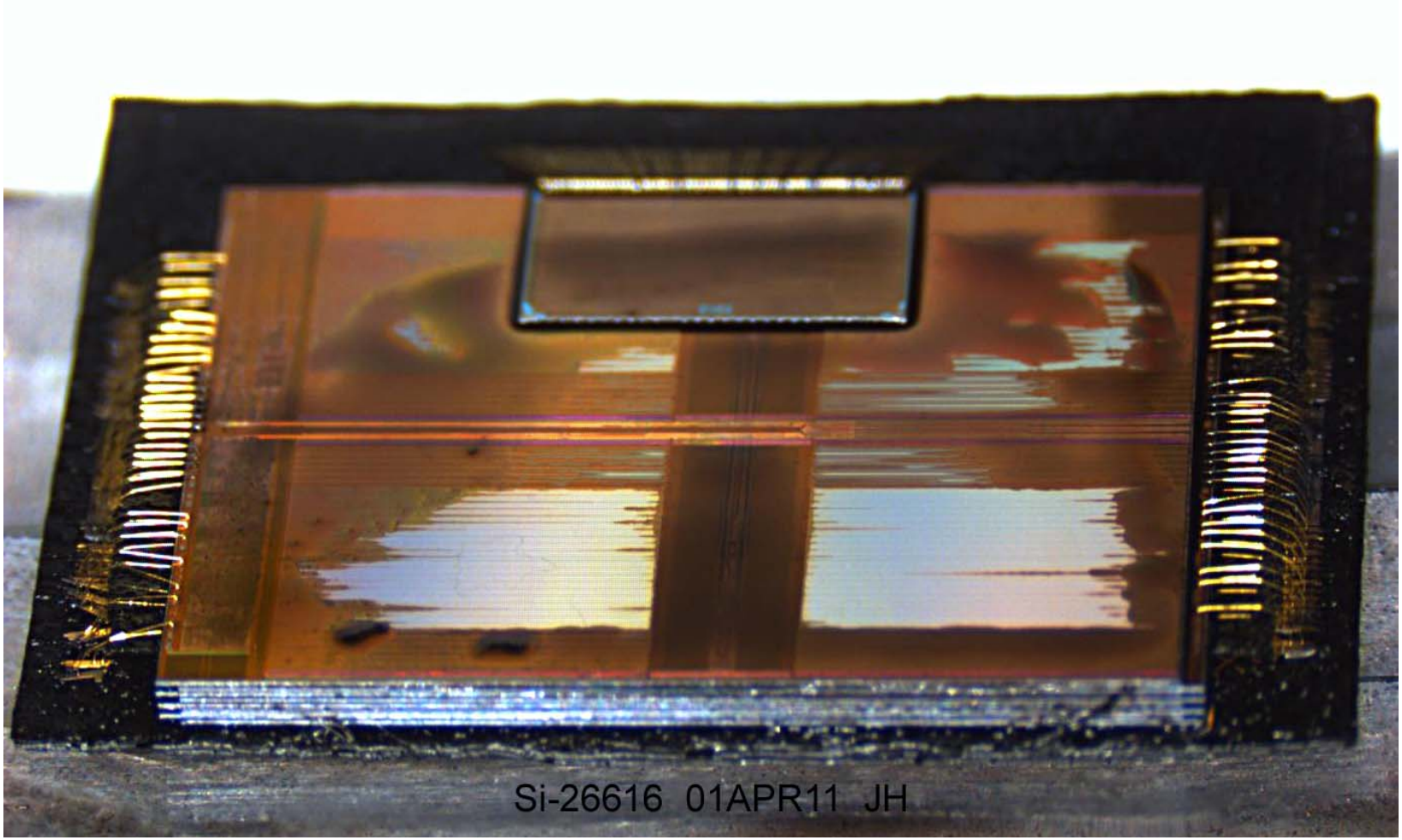


256Gb HLNAND2 E/S in 2011

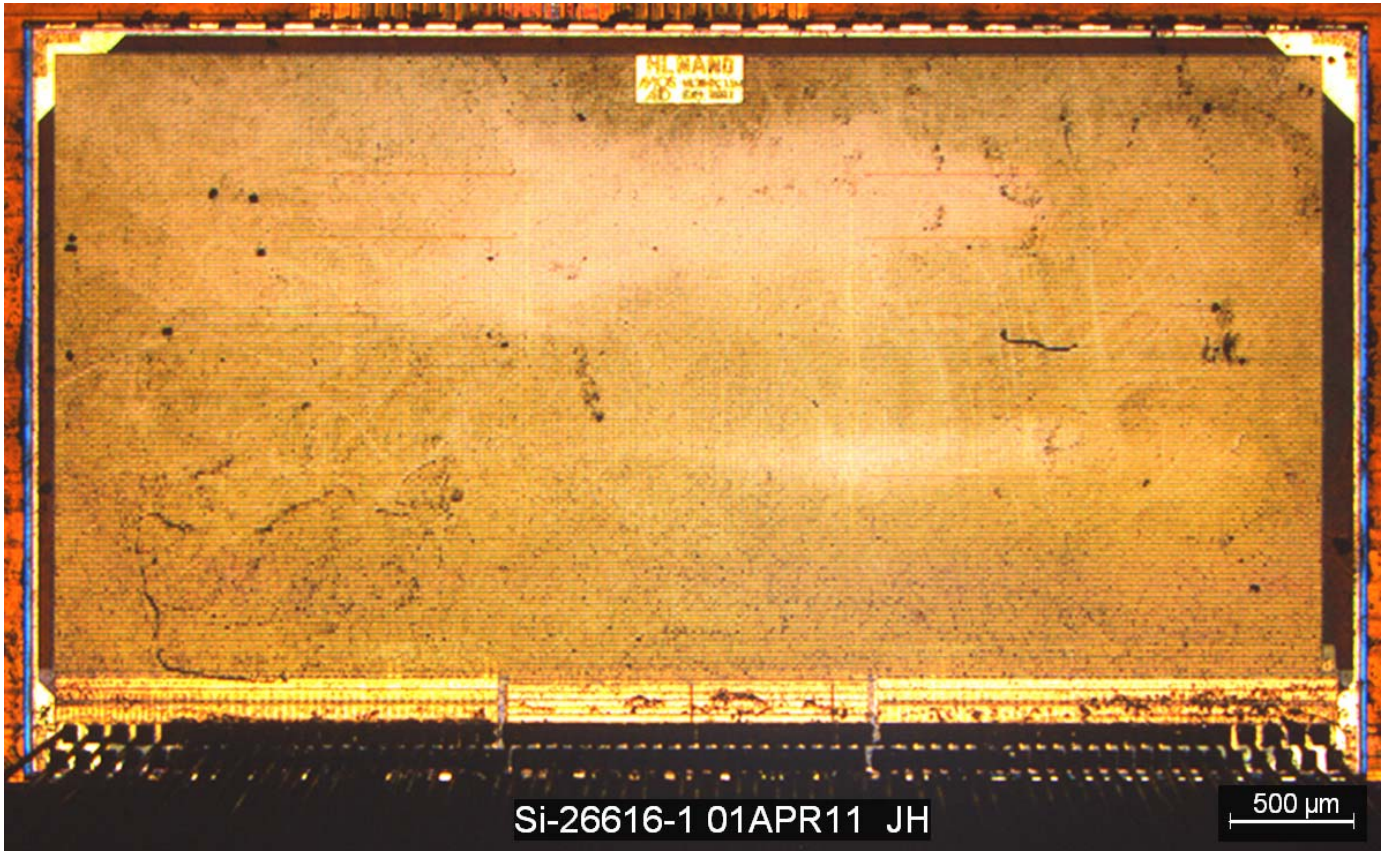
- Achieved fully working engineering sample of 256Gb HLNAND2 in Sep 2011



HLNAND: 9-die Stacked View

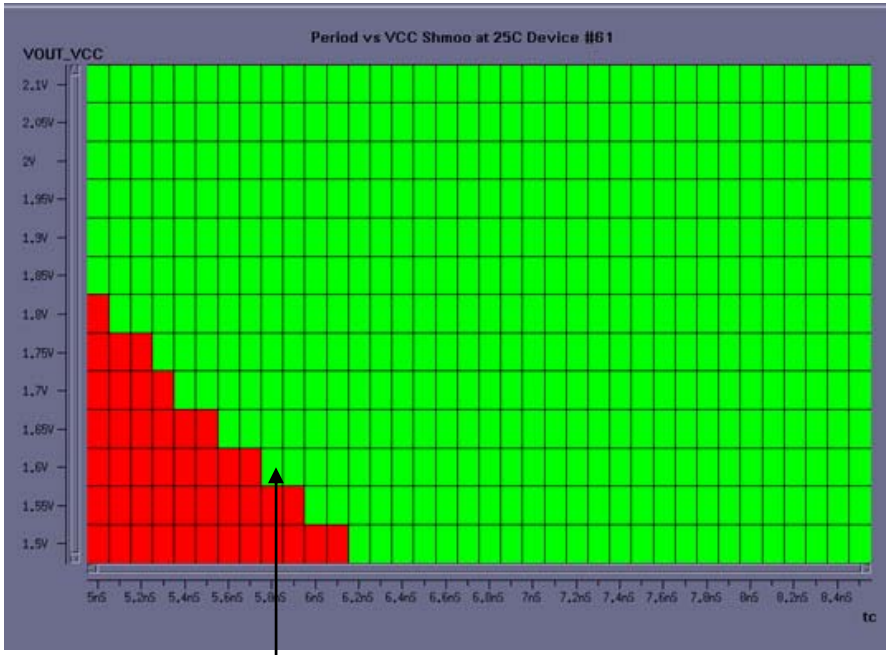


HLNAND Interface Chip



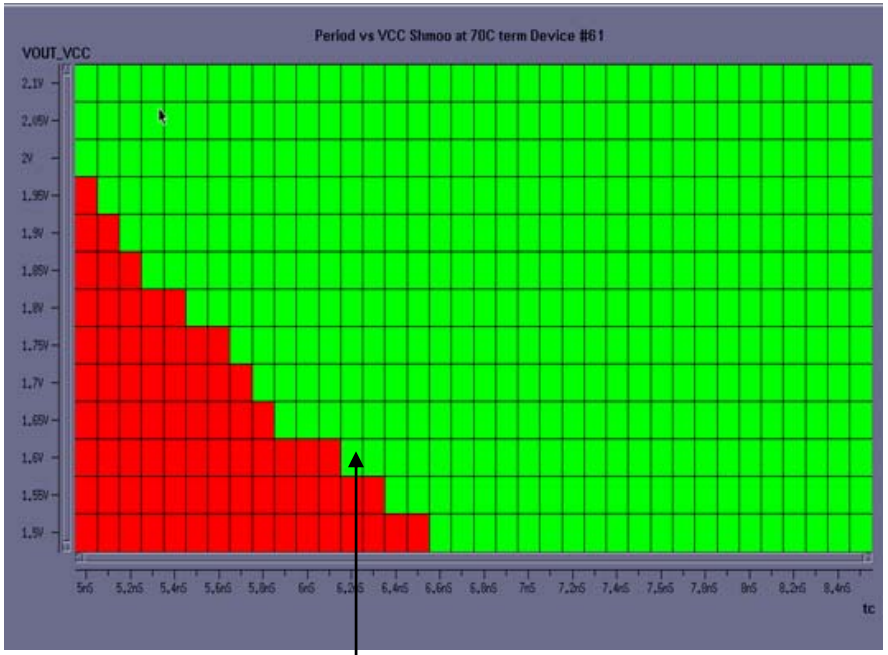
256Gb HLNAND Performance
(DDR266 Grade)

@1.6V and Room Temp.



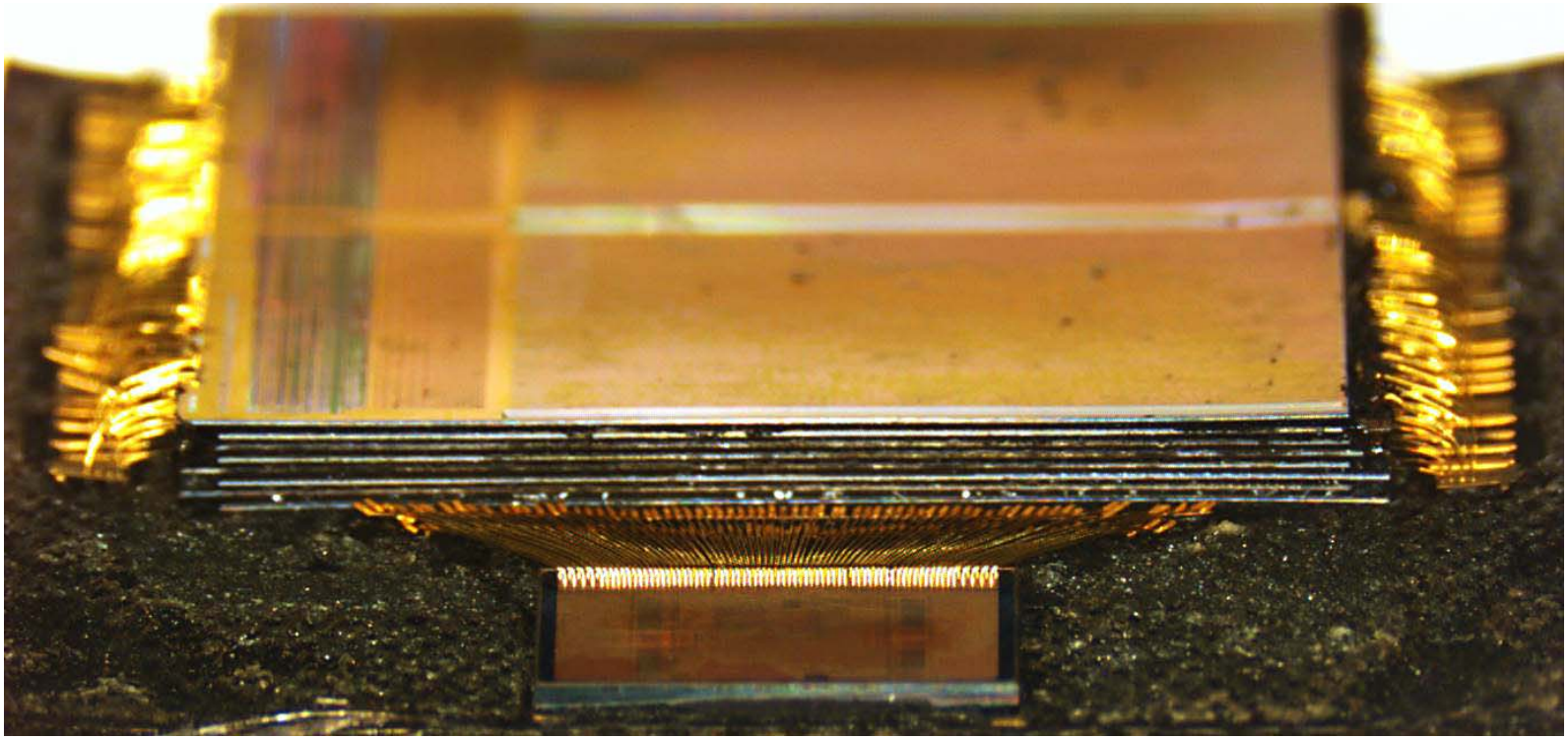
DDR-346 @173MHz

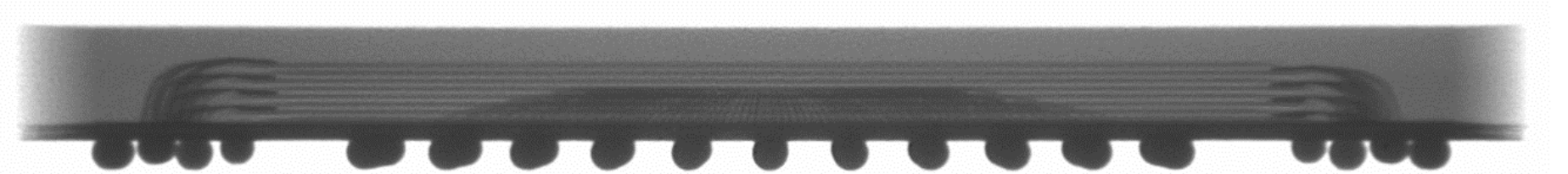
@1.6V and 70°C



DDR-322 @161MHz

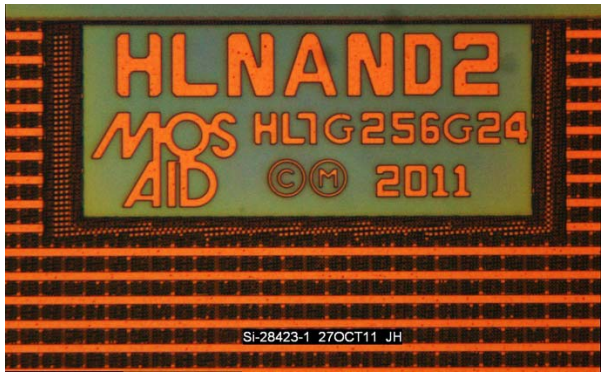
HLNAND2: (8+1)-die Stacked View





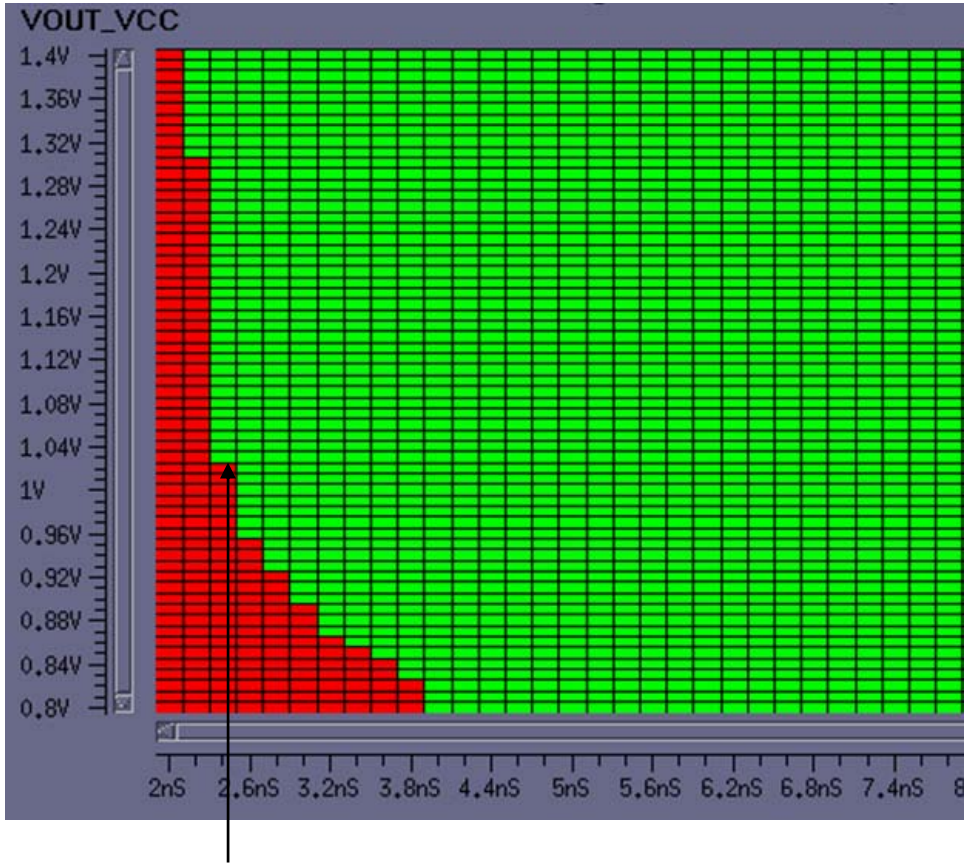
HLNAND2 Interface Chip

- Die Size = 5mm x 2mm = 10mm^2



256Gb HLNAND2 Performance
(DDR800 Grade)

@ Room Temp.



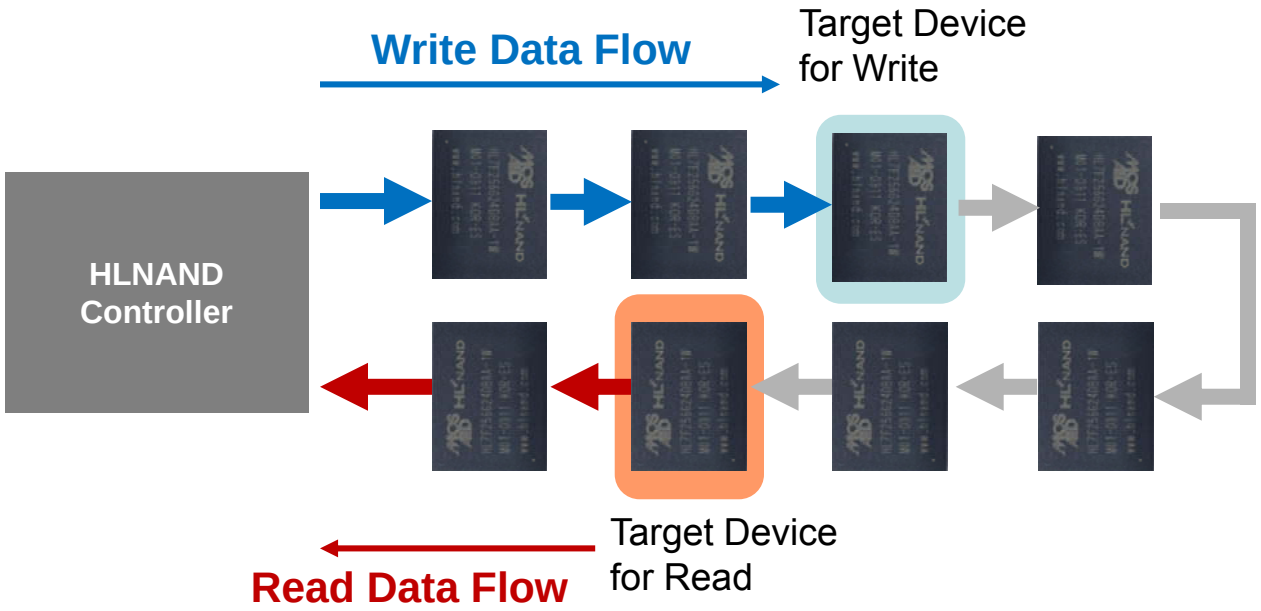
DDR-834 @417MHz

HLNAND/HLNAND2 Key Features

- DuplexRW™ (QDR533/QDR 1600): Simultaneous Read/Write operations, effective 533MBs/1600MBs data throughput
- Built-in EDC (Error Detection Code), on and off control
- Packet truncation for saving power
- Independent automatic status bus - separate status ring (STI/STO)

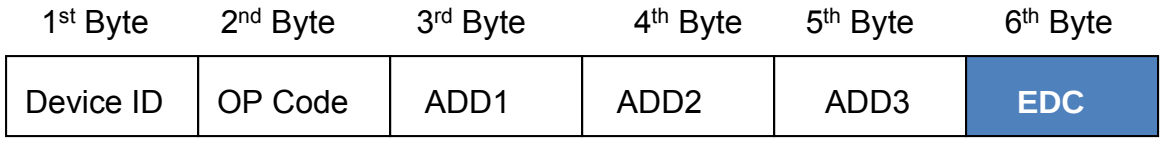
DuplexRW™ (QDR Operation)

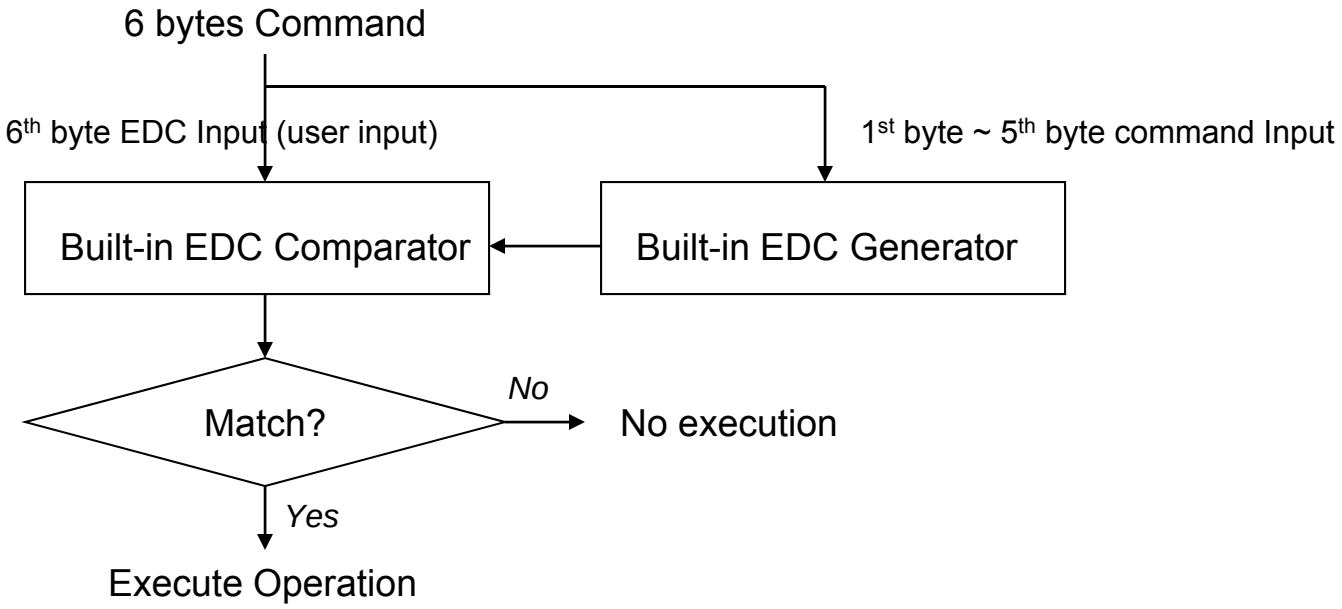
- Simultaneously write to upstream device while reading from downstream device
- Effectively doubles data throughput
  - HLNAND: doubled to 533MB/s
  - HLNAND2: doubled to 1600MB/s



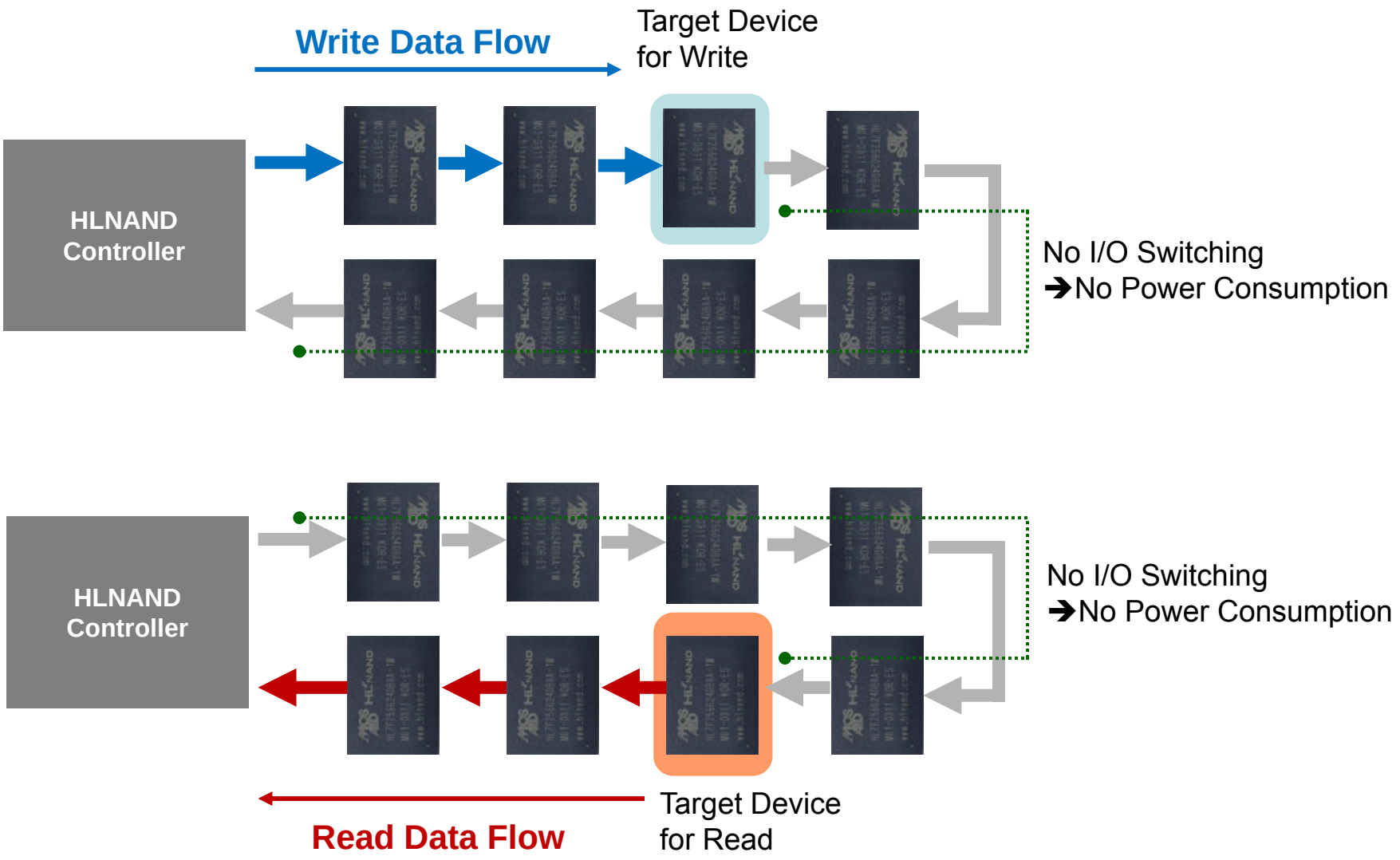
Built-in EDC (Error Detection Code)

6-byte Command Architecture

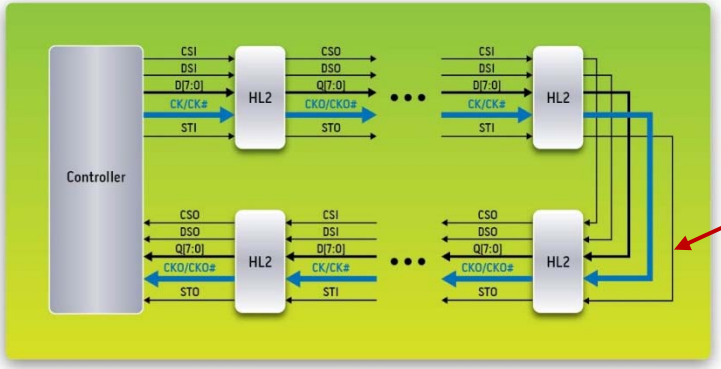




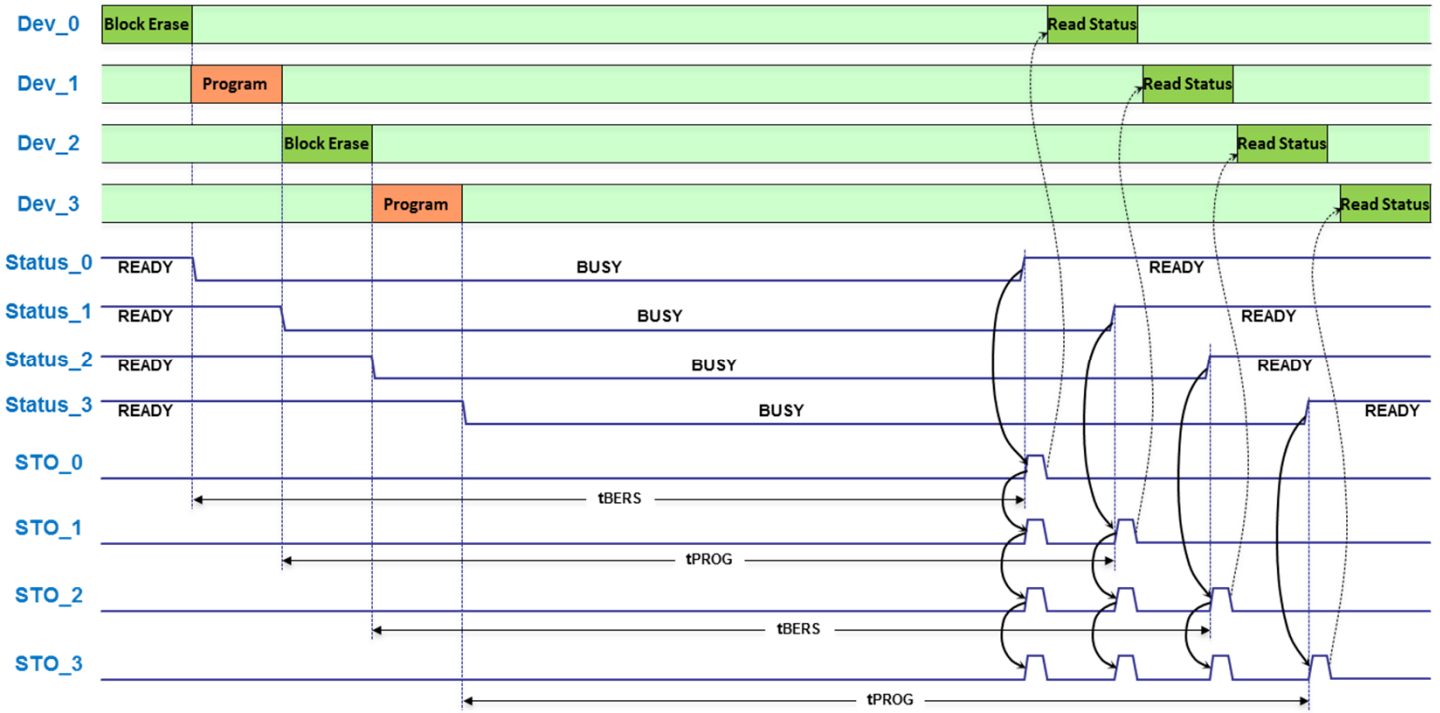
Packet Truncation



Independent Automatic Status Bus



Separate Status Ring (STI/STO)



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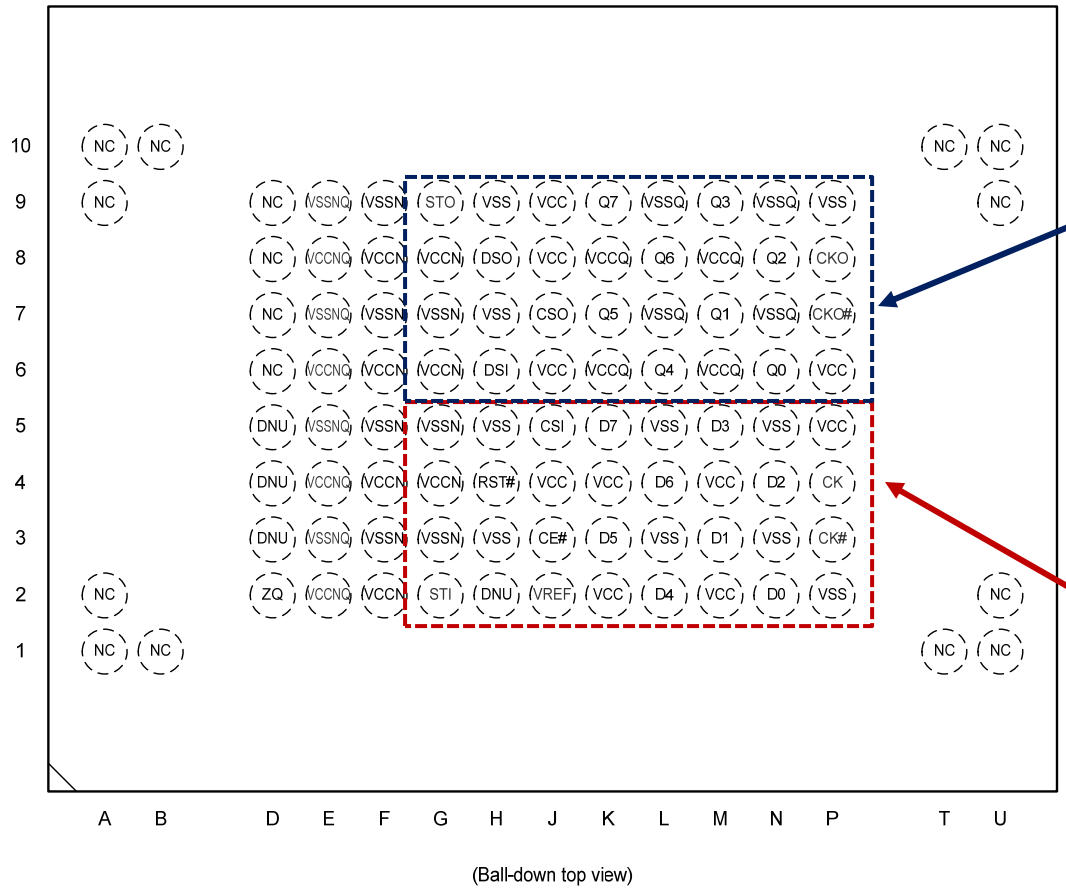
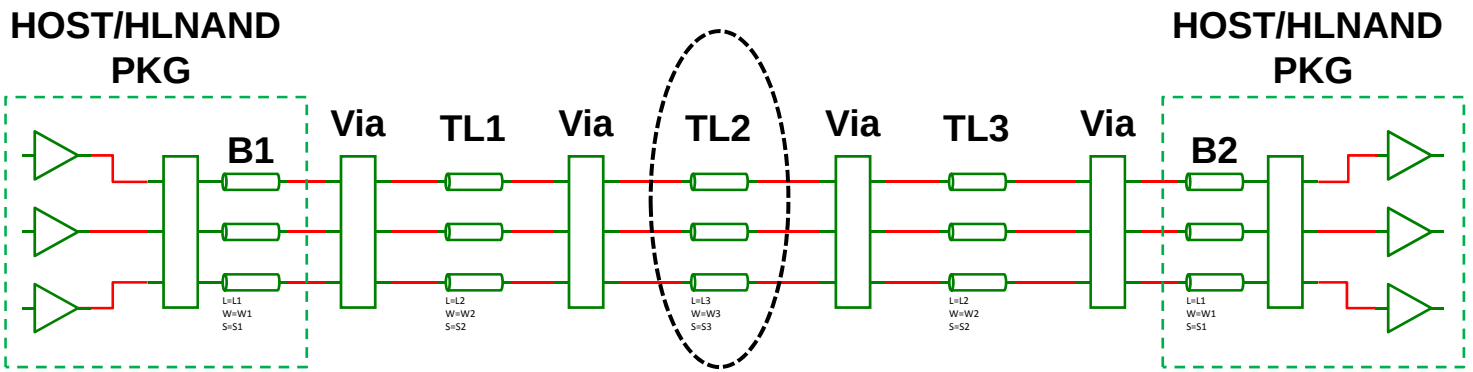
- **Signal Integrity**
- Summary

HLNAND2 Signal Integrity
(Signal to Ball Assignment)

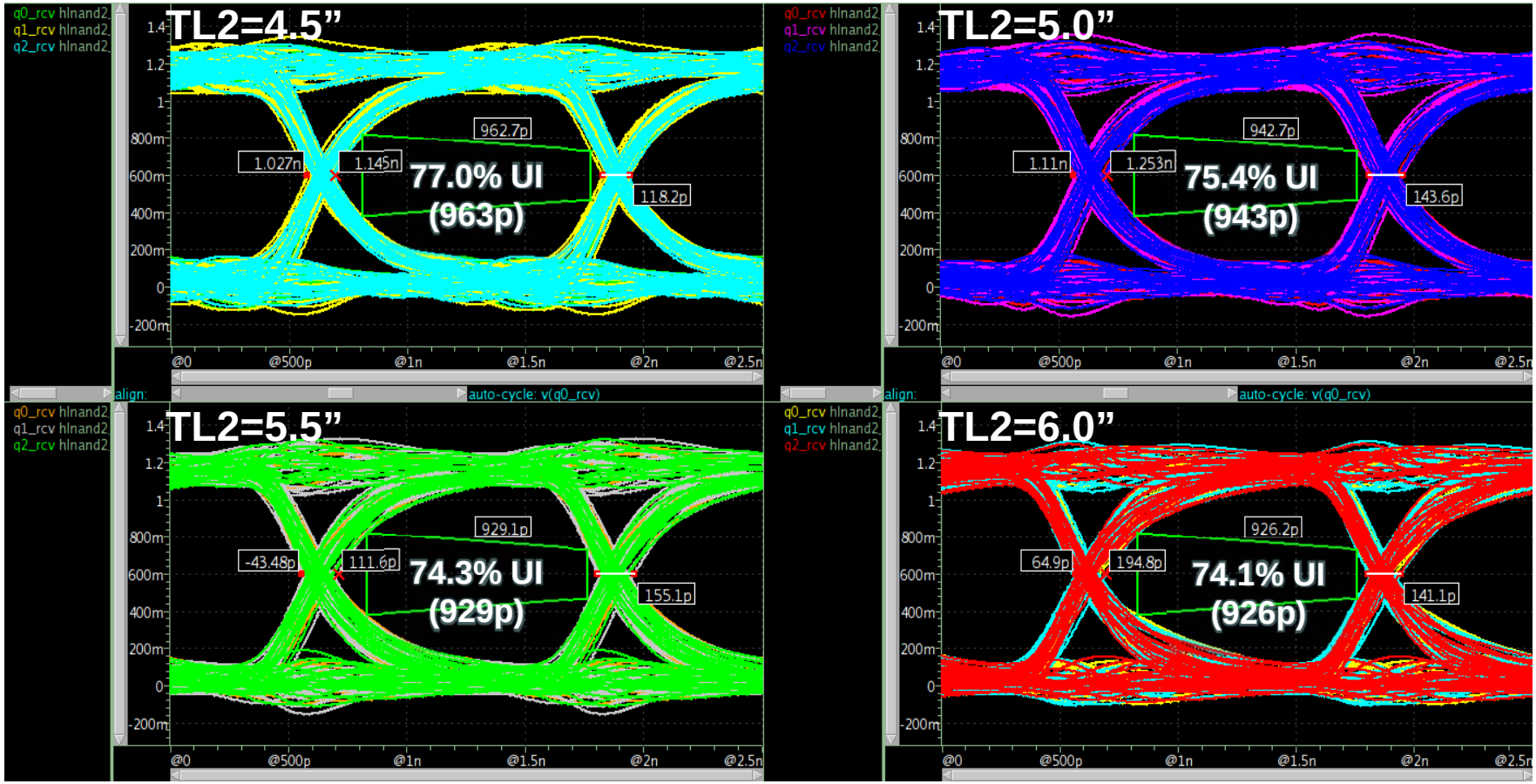


HLNAND2 Signal Integrity
(General Topology Model)

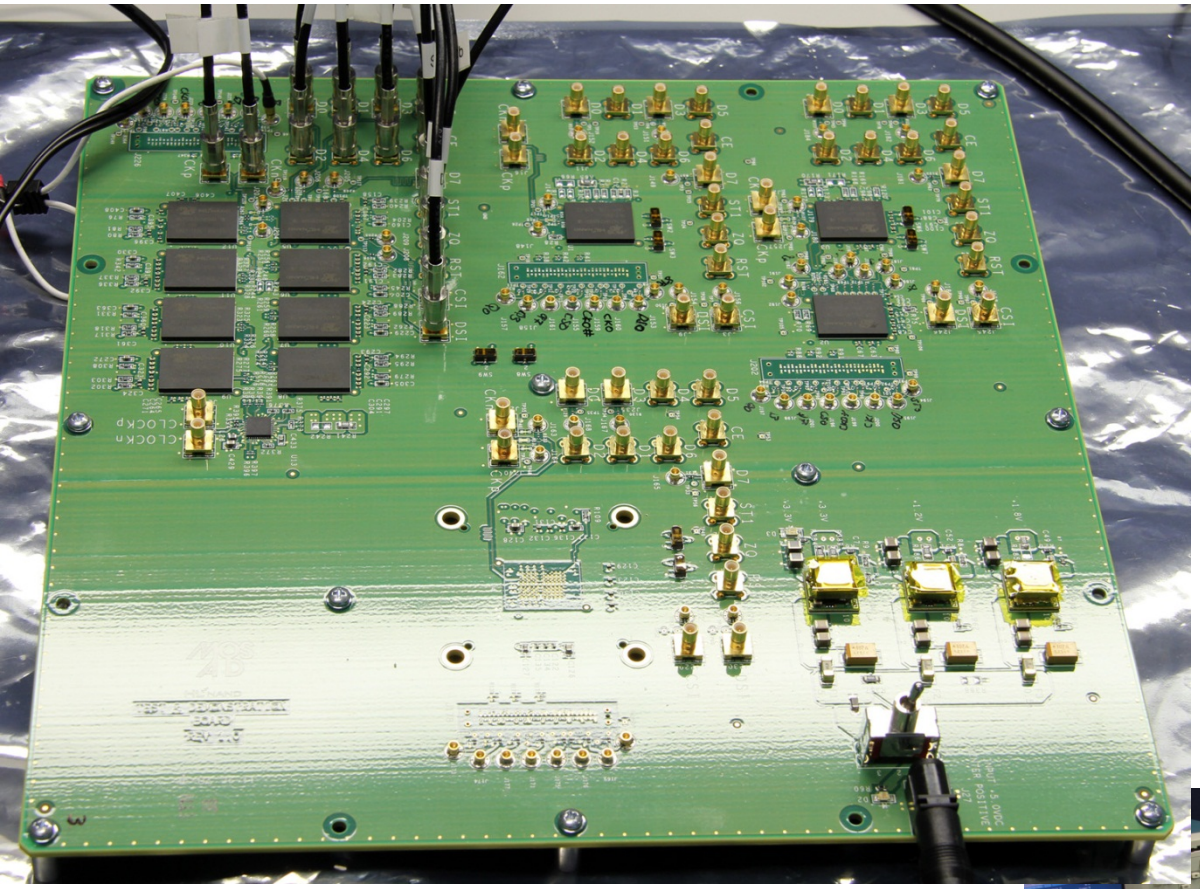


- 3 Line Model for X-talk
- PCB Impedance = 50 Ω ± 7.5 Ω
- Space of Lines = 4 and 8 mil
- Min. time width of RCV eye window = 0.66UI
- Driver Strength = 50 Ω
- ODT is not required

HLNAND2 SI Simulation
(DDR-800 Point-To-Point, No Termination)

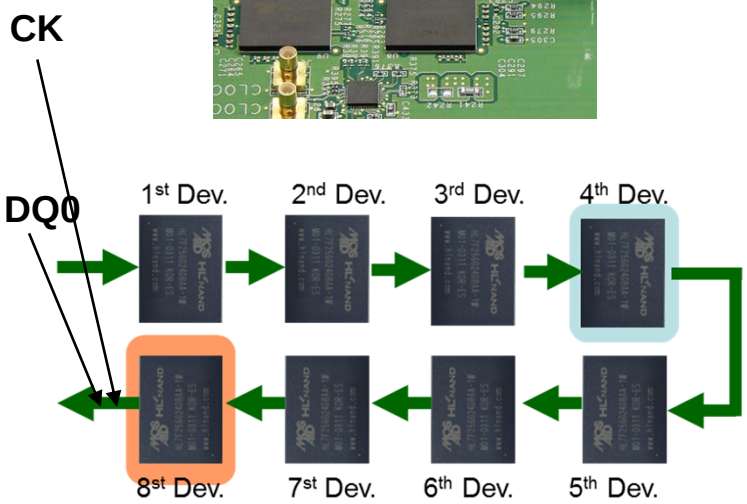


HLNAND2 Test Board

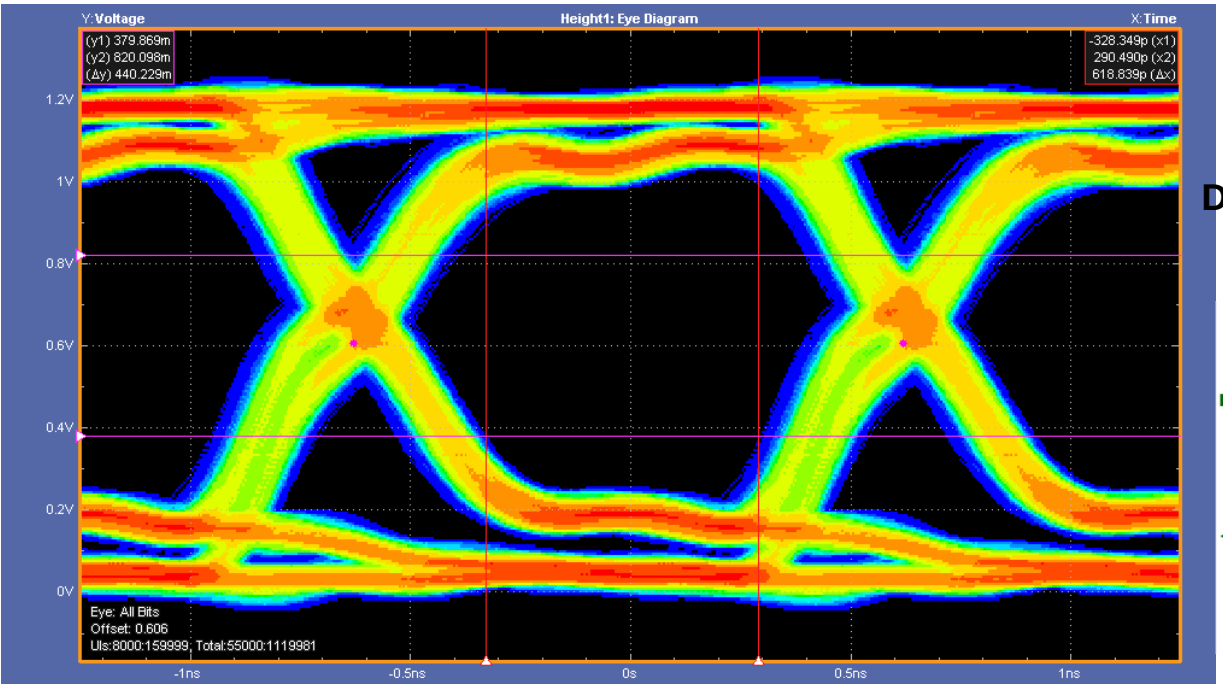


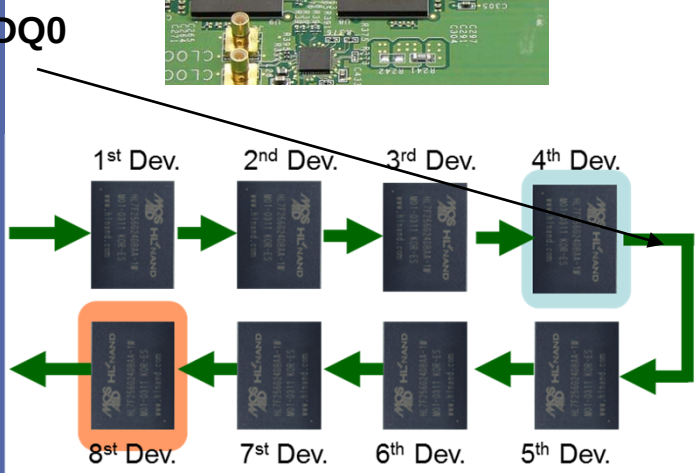
Measured Signal

(CK Output/DQ Signals from 8th Dev. @DDR800)



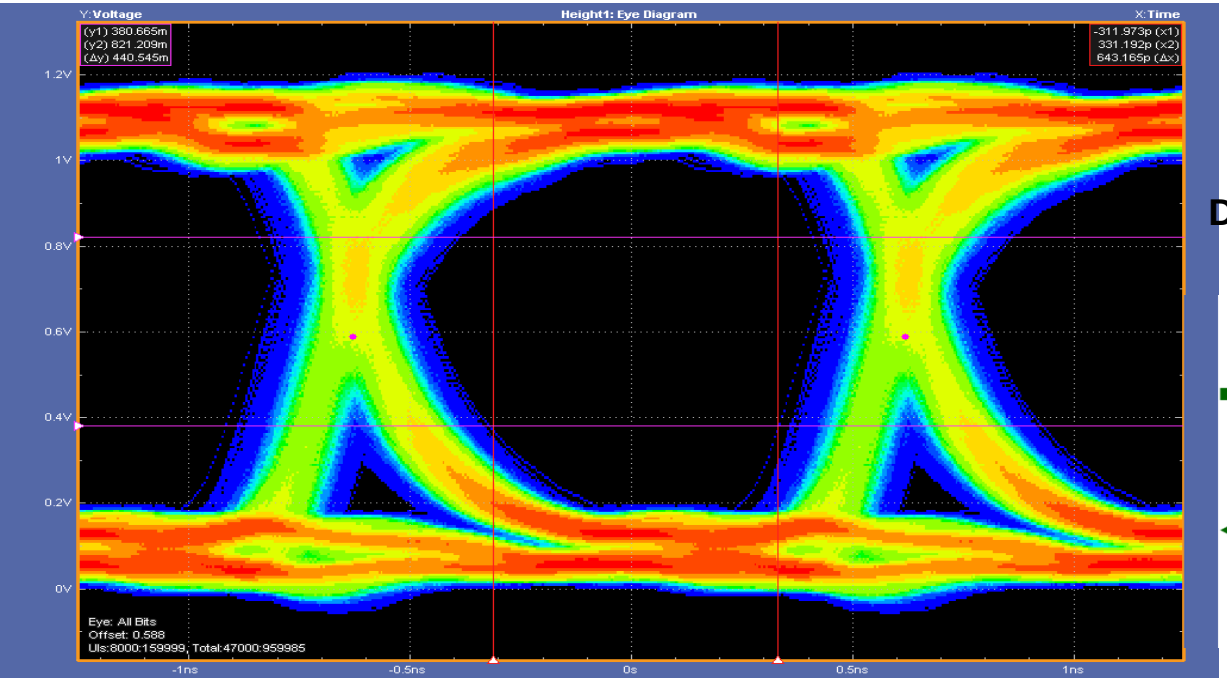
Measured Data Eye
(DQ Signals from 4th Dev. @DDR800)

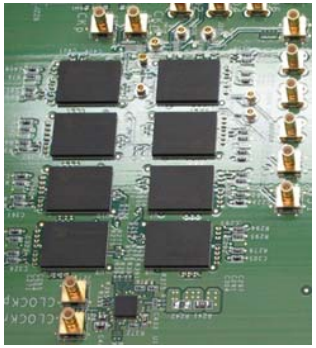


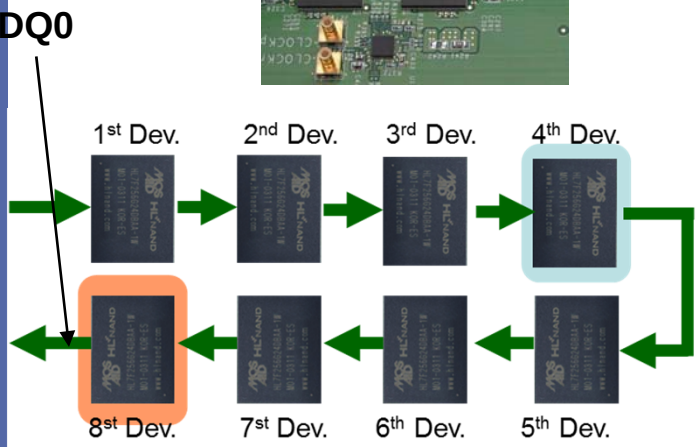


Measured Data Eye
(DQ Signals from 8th Dev. @DDR800)

DQ0 (Data Eye)







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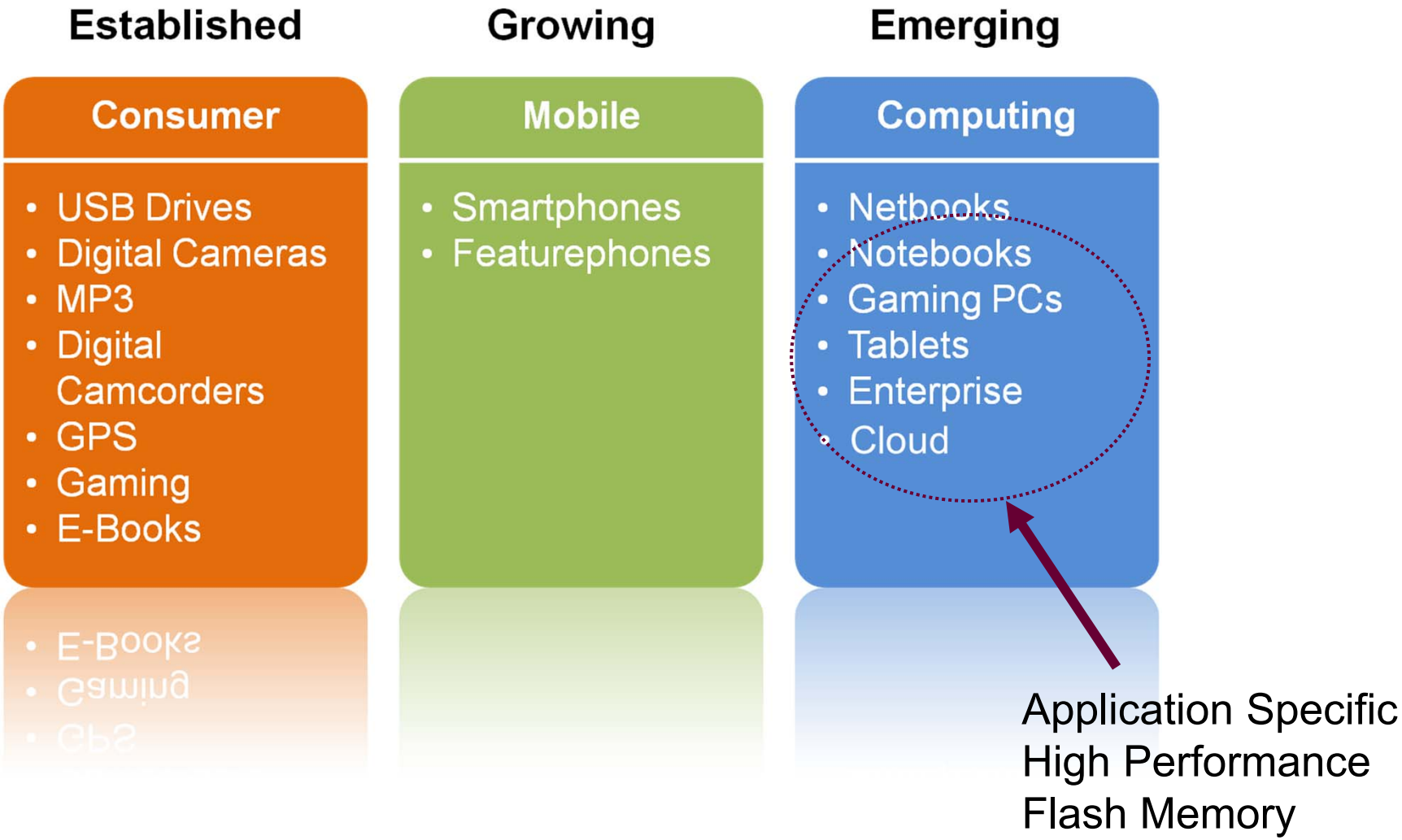
HLNAND Target Market

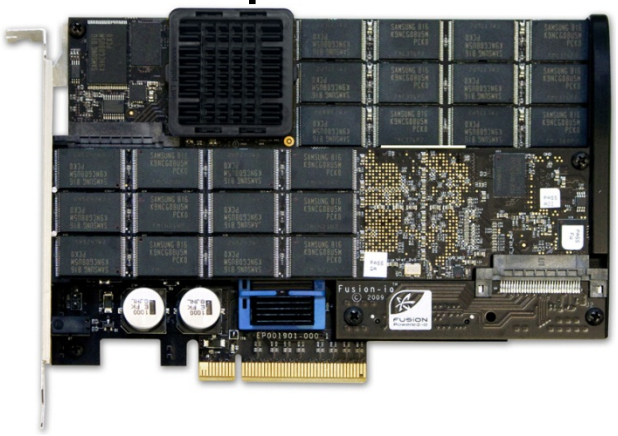


HLNAND Applications

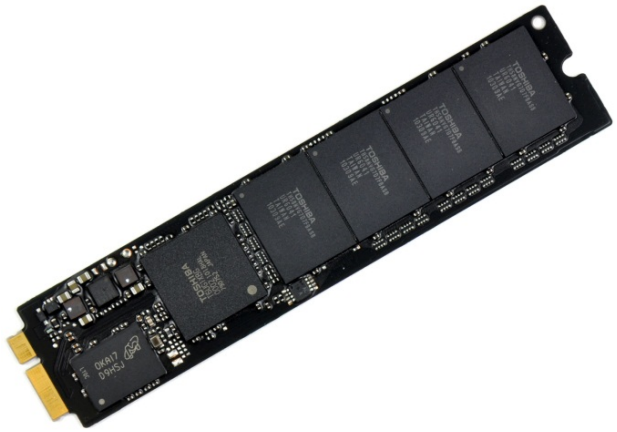
Consumer SSD

Embedded Flash

Enterprise SSD

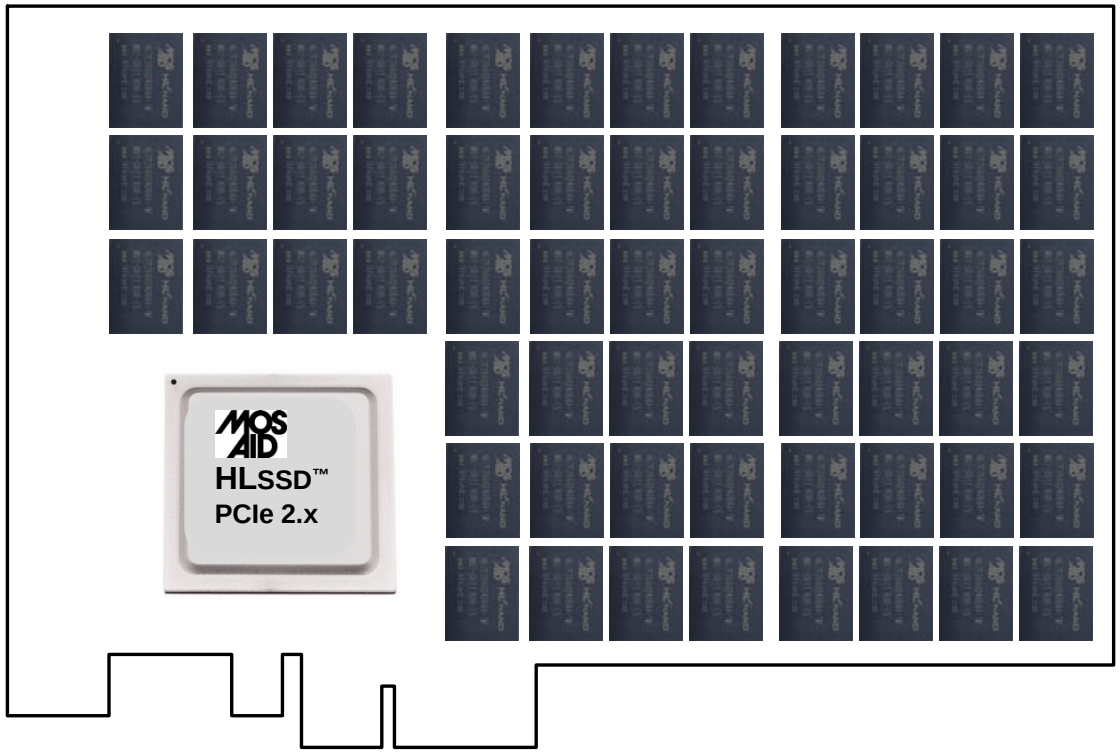


SSD Modules



HLSSD Development

- Native PCIe Flash Controller (ASIC/FPGA)
- X4 or x8 PCIe Gen2/Gen3
- TB Capacity
- GB/s-Performance



HLNAND Flash Benefits

- **Higher Performance**
- **Longer System Longevity***
- **Lower Power Consumption**
- **High Scalability**
- **Interface Extensibility**
- **Advanced Features**
- **Reduced Overall Cost**

* Monolithic HLNAND

Resource for HLNAND Flash

www.HLNAND.com