Developing a Prototyping Board for Emerging Memory

2013. 10. 25

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POSTECH

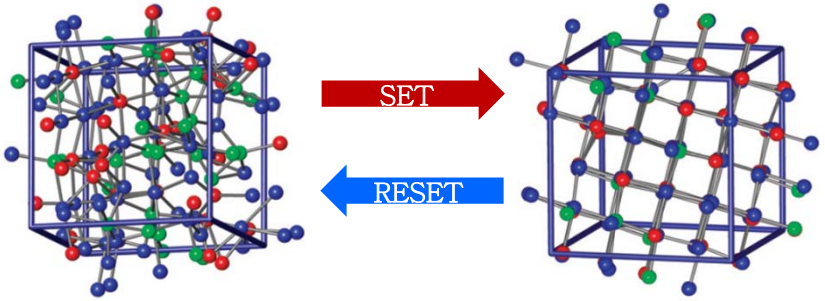
Introduction

- DRAM scaling problem

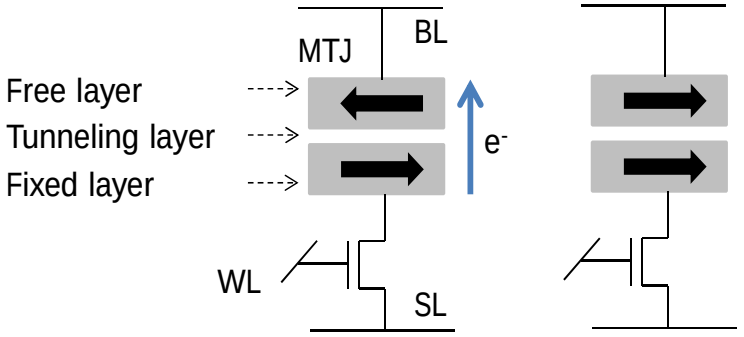
[ITRS, 2012]

Year	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
DRAM 1/2 Pitch (nm)	31	28	25	22	20	18	16	15	13	12
Manufacturable solution	Exist	Known				NOT Known				
STT-MRAM tech. node (nm)	65	45	45	45	32	32	32	22	22	22
Manufacturable solution	Exist									
PCRAM tech. node (nm)	38	32	28	24	21	18	16	14	13	12
Manufacturable solution	Exist									

- Phase-change RAM (PRAM) and Spin-transfer torque RAM (STT-RAM) are candidates



Amorphous = high resistivity Crystalline = low resistivity



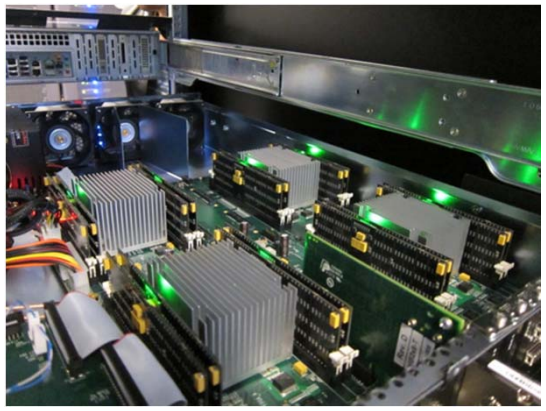
(a) anti-parallel (b) parallel

Why Prototyping Board for New Memory?

- Key benefits of prototyping system are
  - Full software execution, fast speed (w.r.t. simulation models), and closing the gap between models and real devices
- Gap between simulation models (or simple emulations) and real new memory designs
- PRAM case
  - Real PRAM chips do not support bank parallelism in write operations due to peak write current limit
  - Longer write latency (~20μs) than what most models assume (200-300ns)

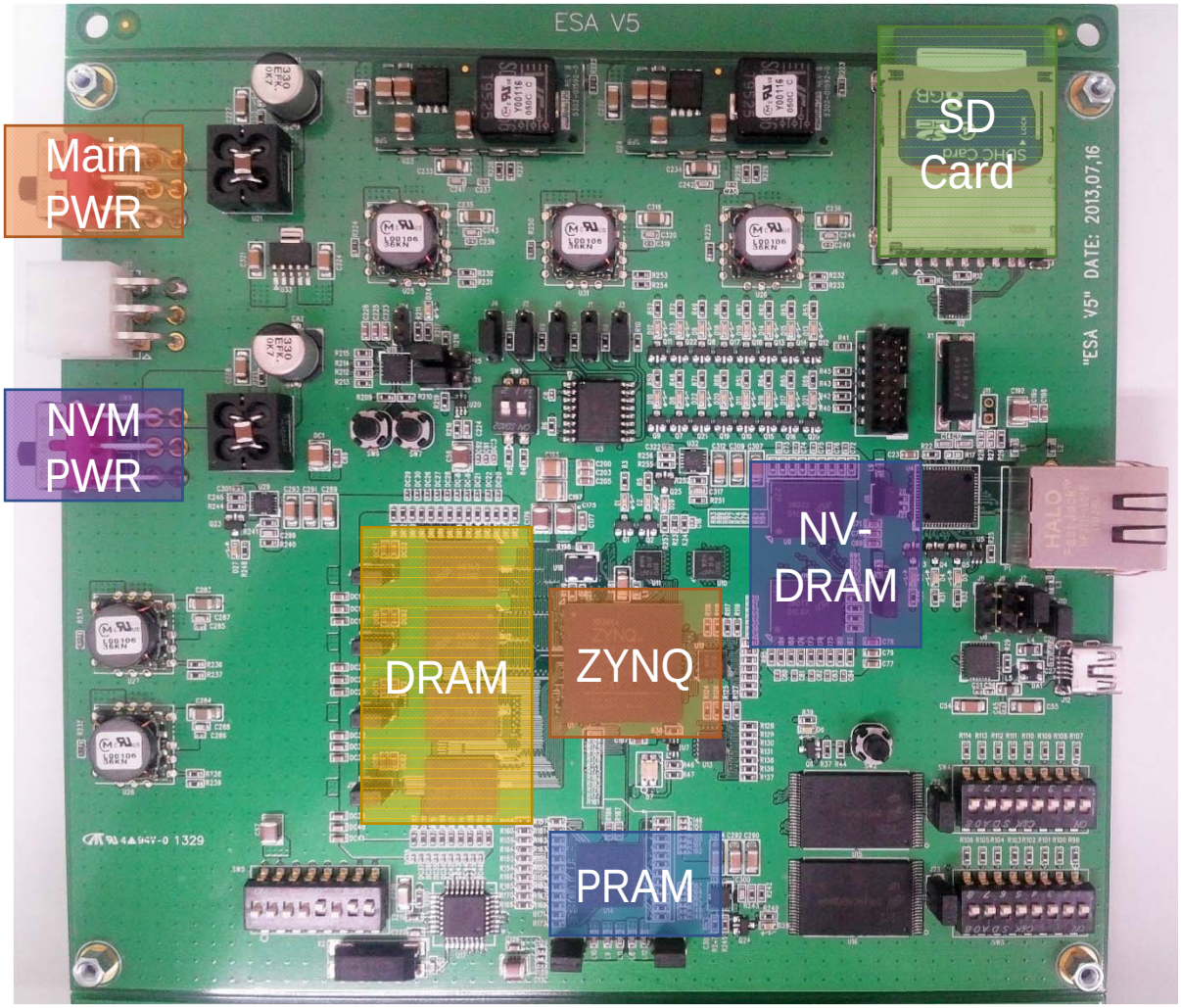
Existing Work

- ONYX [UCSD, 2011]

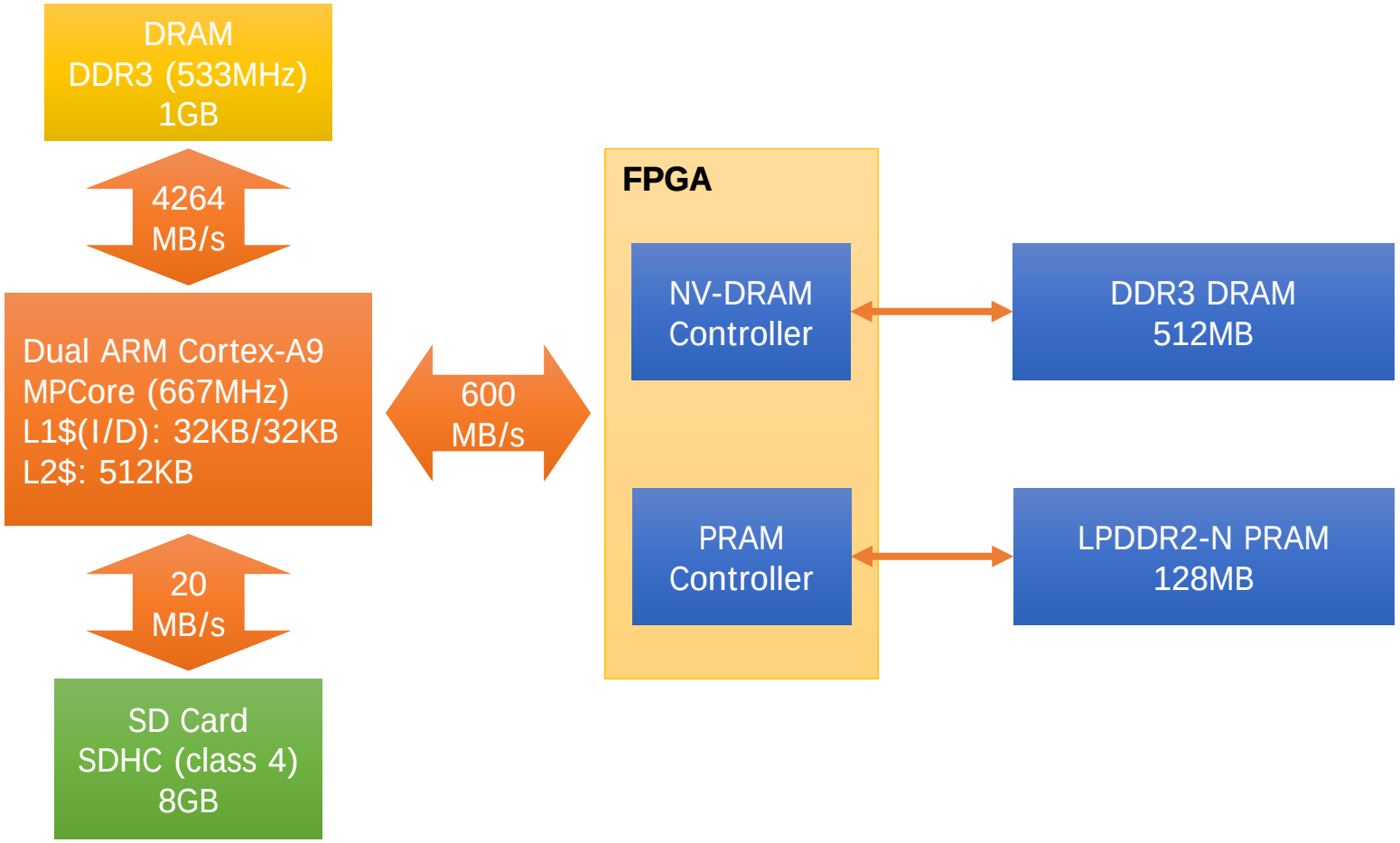


- A ring-based storage array architecture and real hardware implementation
- Targeted at server system storage

Prototyping Board (ESAv5)



Key Components



Board Functions

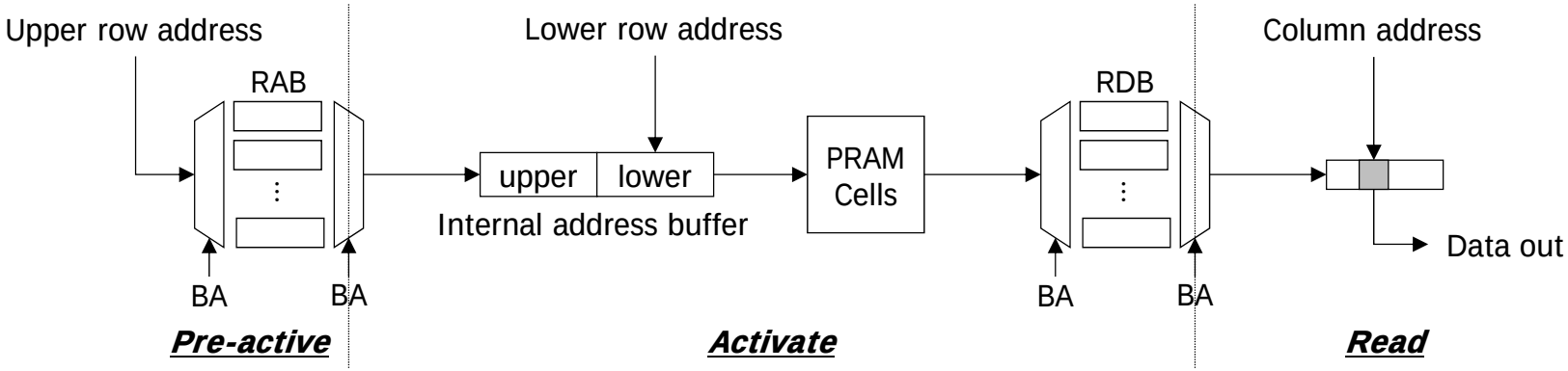
- Linux booting from SD card
- Address map
  - Physical address is allocated to DRAM, PRAM and NV-DRAM through AXI bus

0x0000_0000 – 0x3FFF_FFFF (1GB)	DRAM
0x4000_0000 – 0xBFFF_FFFF (2GB)	PRAM (128MB) NV-DRAM (512MB)

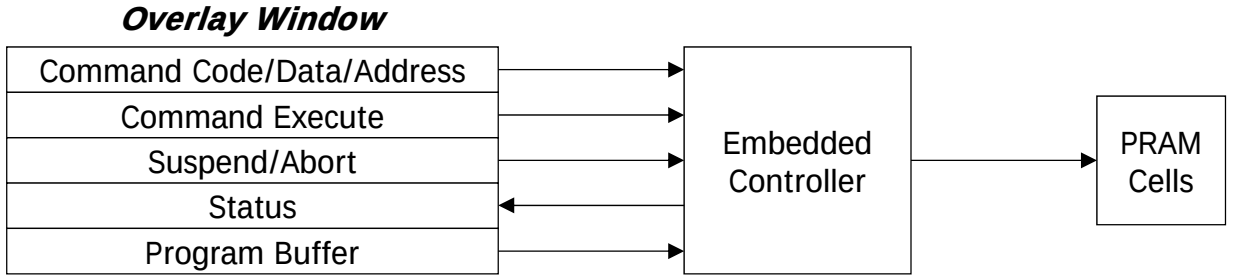
- Key features
  - Real PRAM chip usage
  - STT-RAM emulation (with DRAM)
    - Latency emulation
    - Non-volatility

Read and Write Paths in PRAM

- LPDDR2-NVM interface (JEDEC standard)
  - Read Path

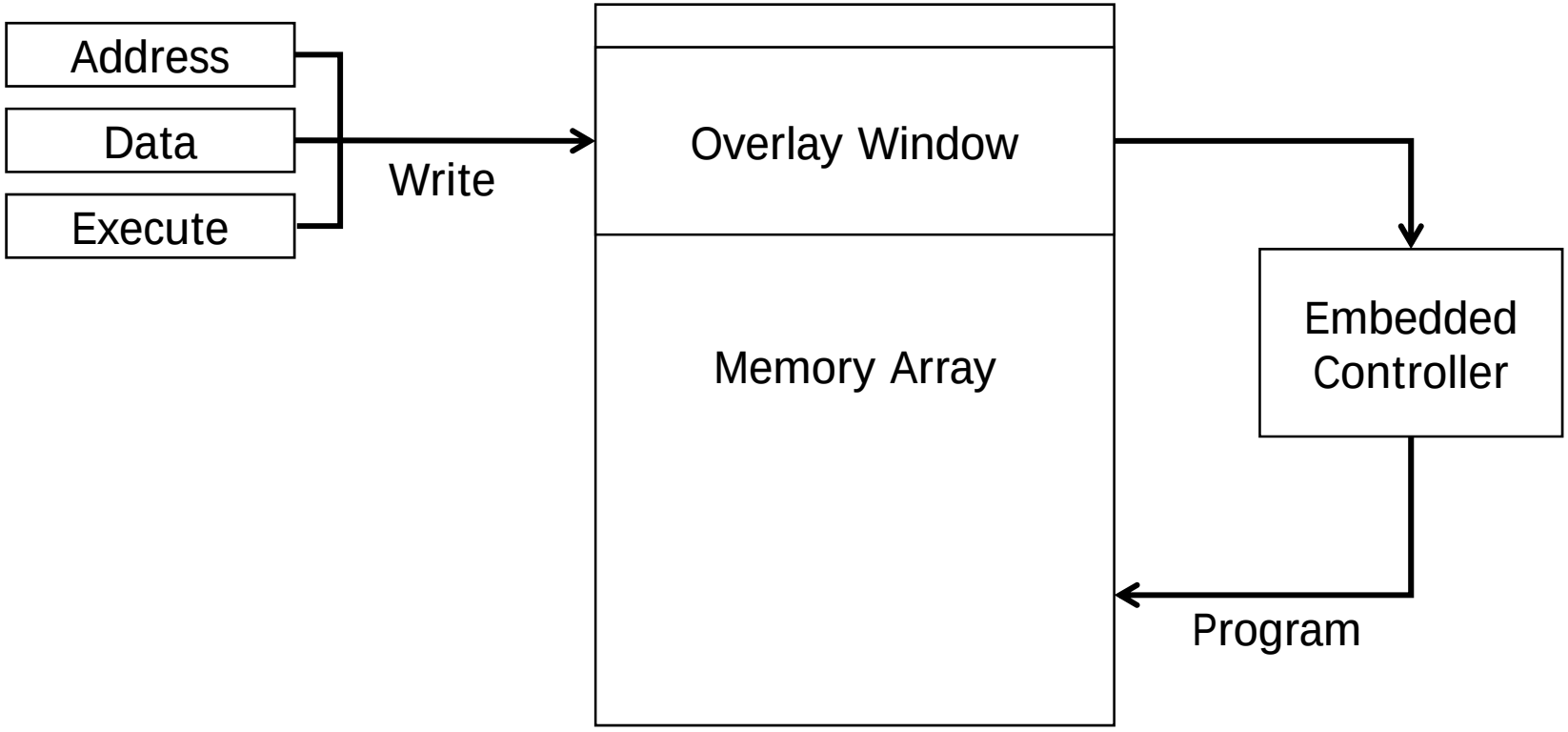


  - Write Path



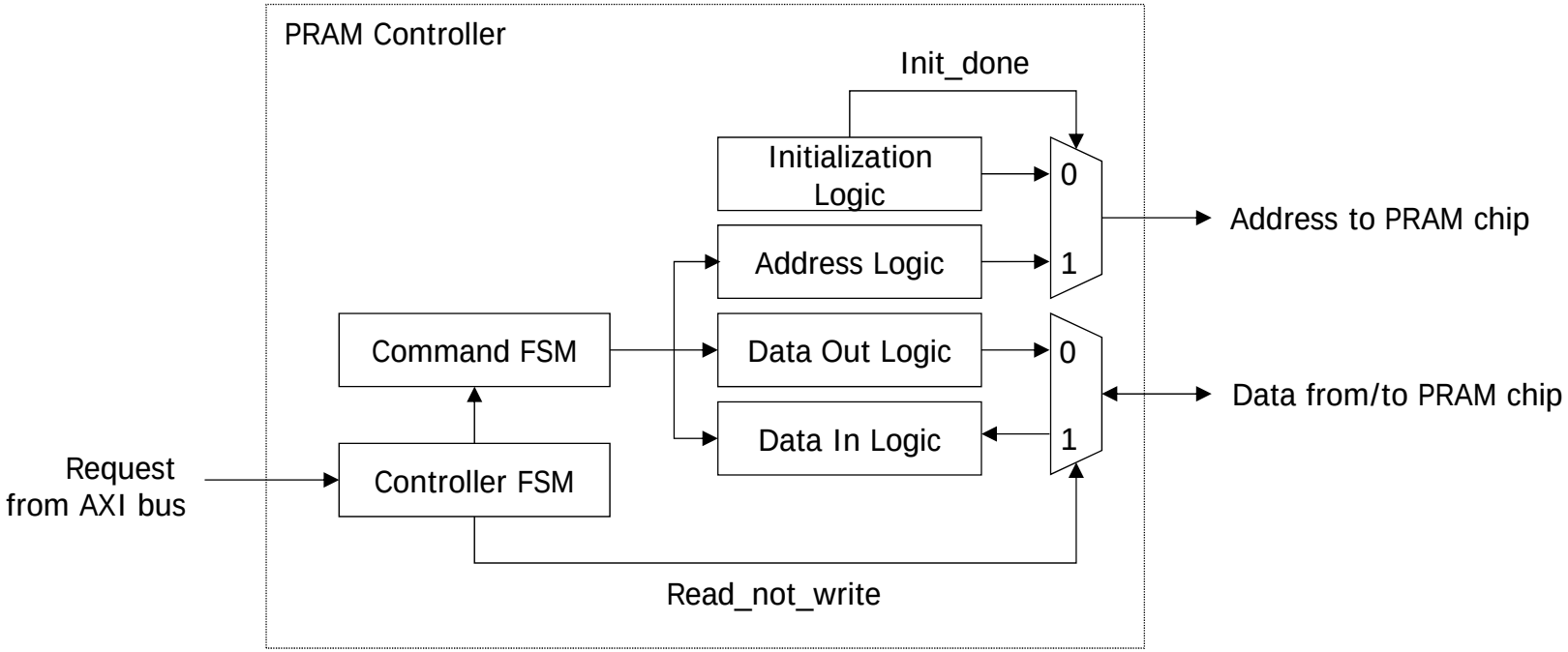
Program Operation using Overlay Window

- Overlay window contains program buffer and control/status registers



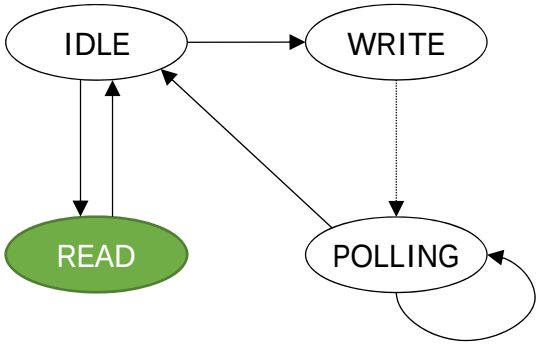
PRAM Controller

- Block Diagram

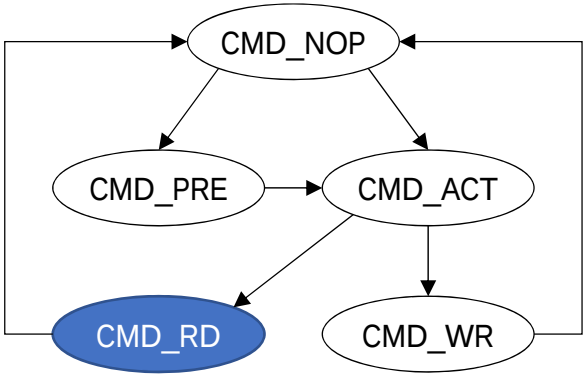


PRAM Controller

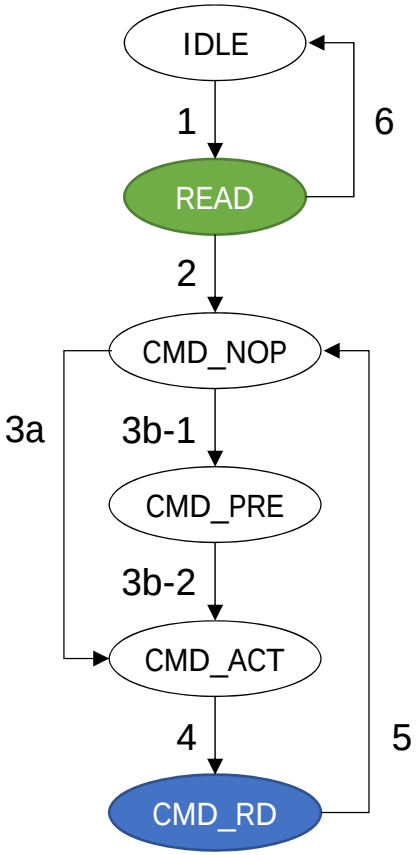
- Controller FSM



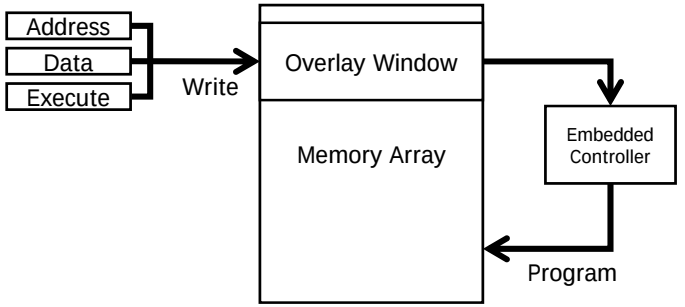
- Command FSM



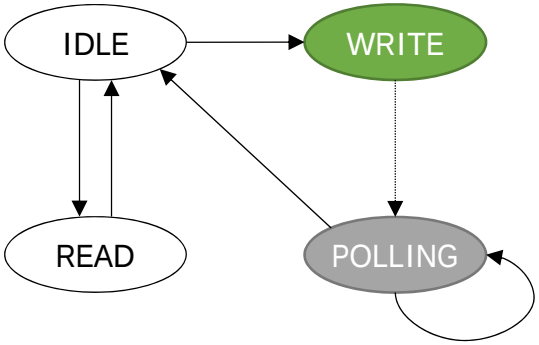
Read Request



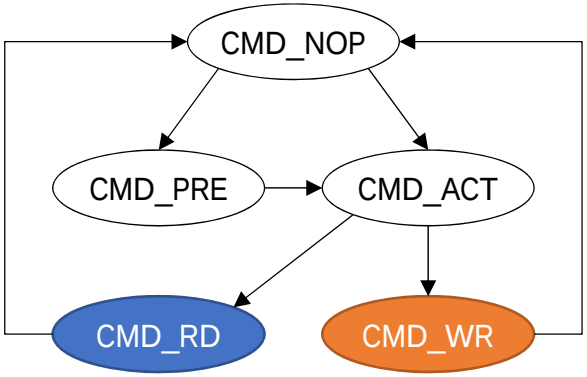
PRAM Controller



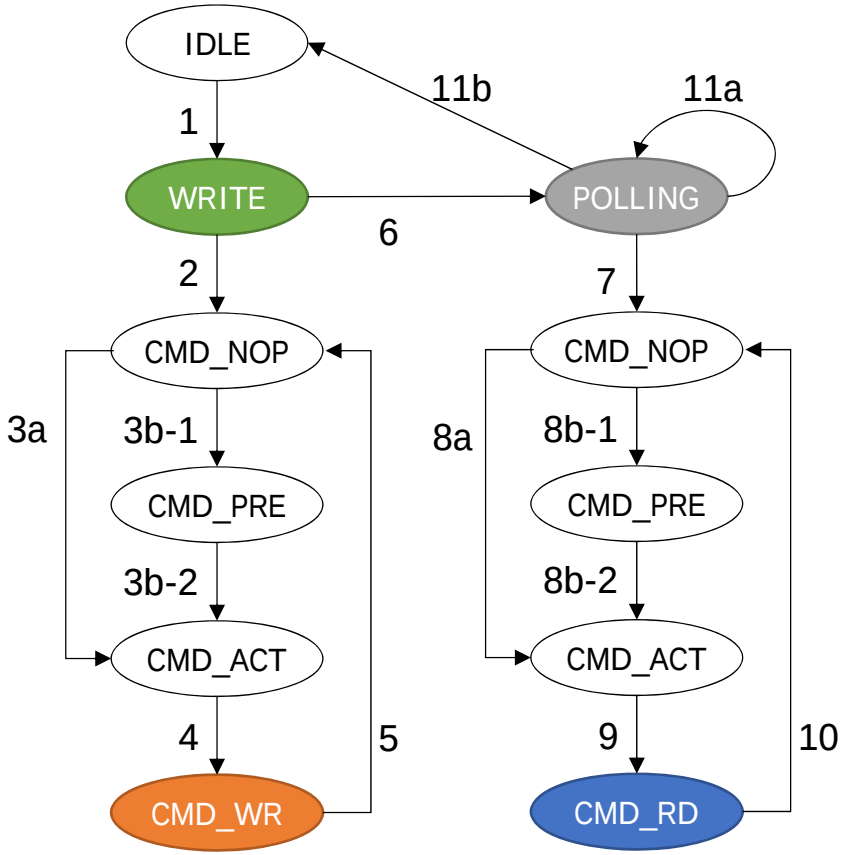
- Controller FSM



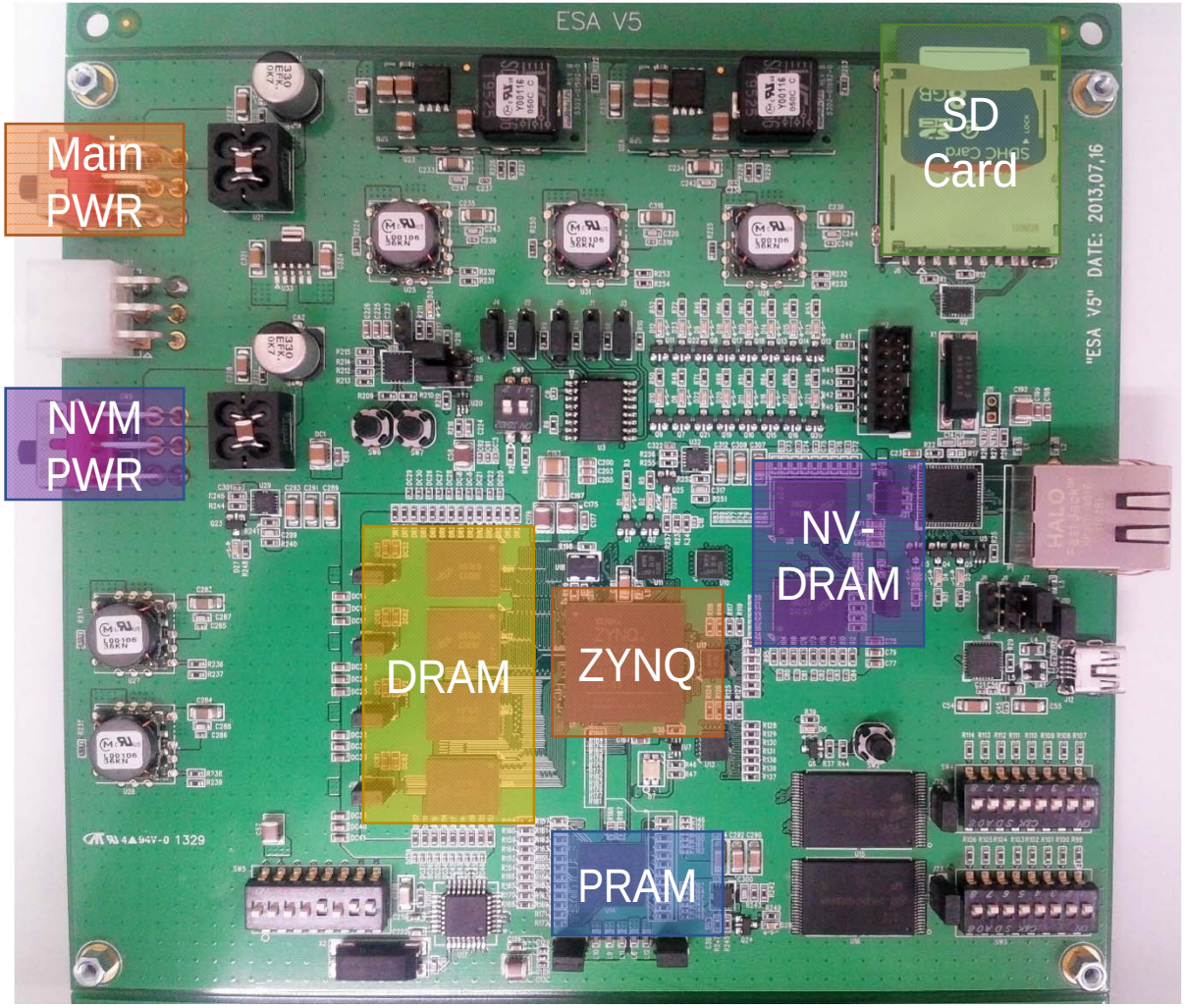
- Command FSM

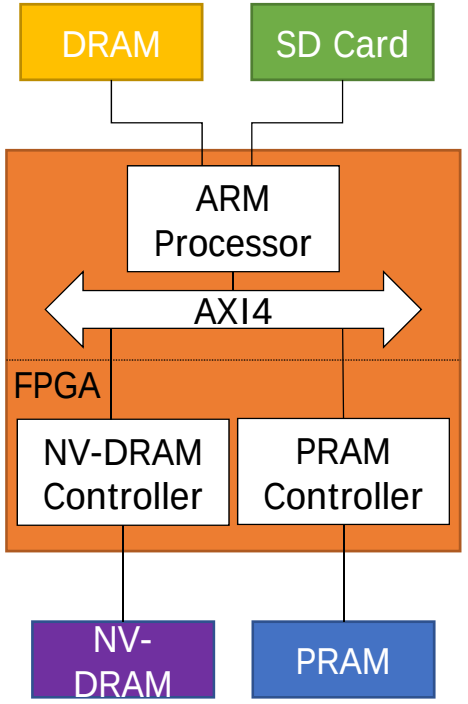


Program opration



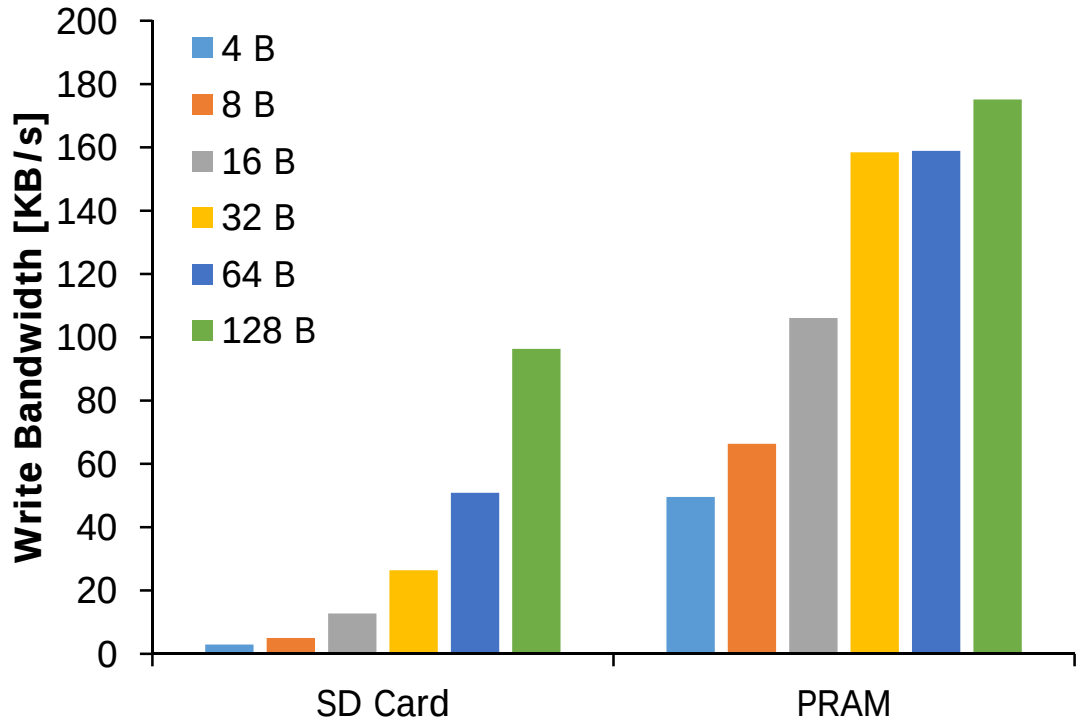
SD Card vs PRAM





Write Bandwidth Comparison: SD card vs PRAM

- PostMark



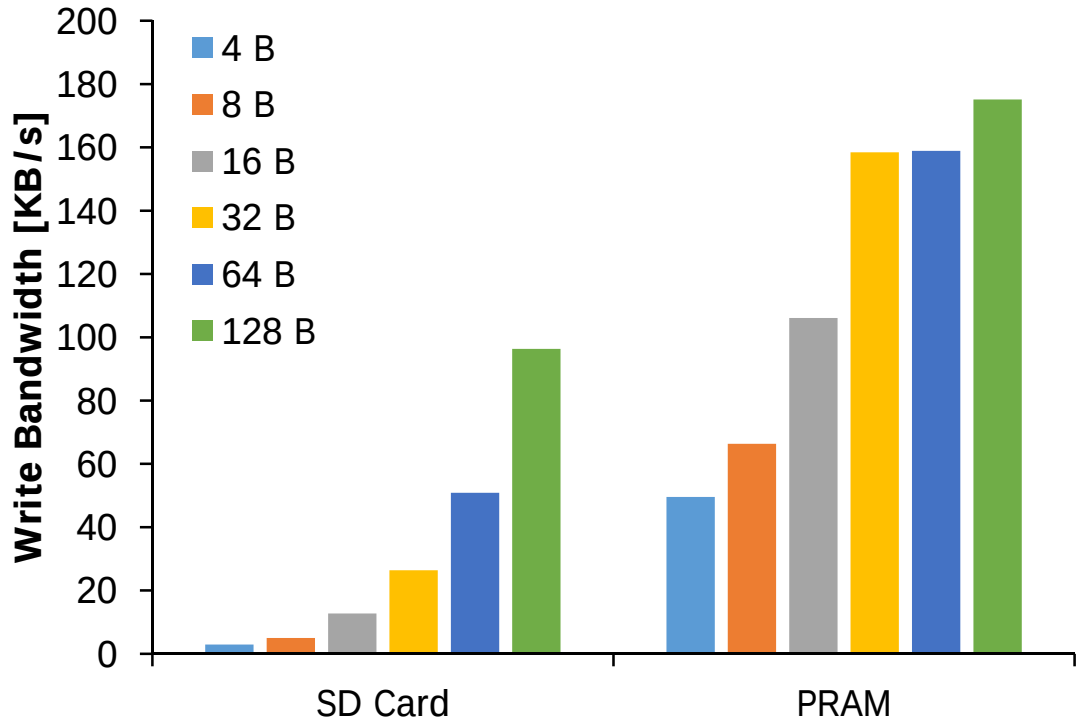
Modified PostMark for PRAM by replacing functions

SD Card	PRAM
`fopen()`	`mmap()`
`fread()` `fwrite()`	`memcpy()`

*mmap for PRAM usage
va_pram = mmap(/dev/mem, OFFSET);

Write Bandwidth Comparison: SD card vs PRAM

- PostMark



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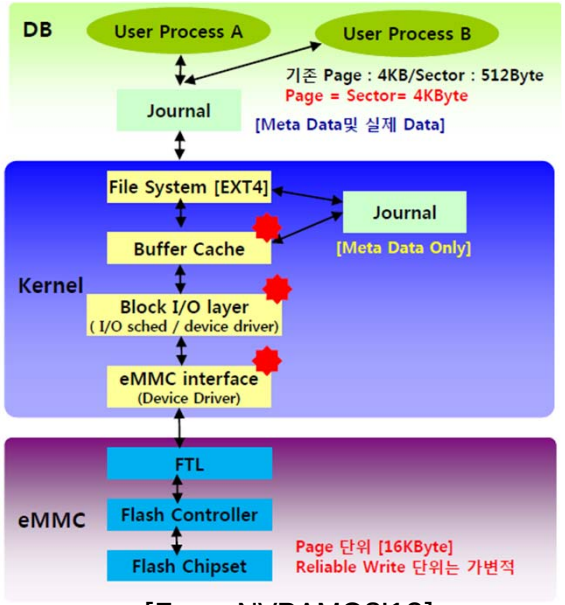
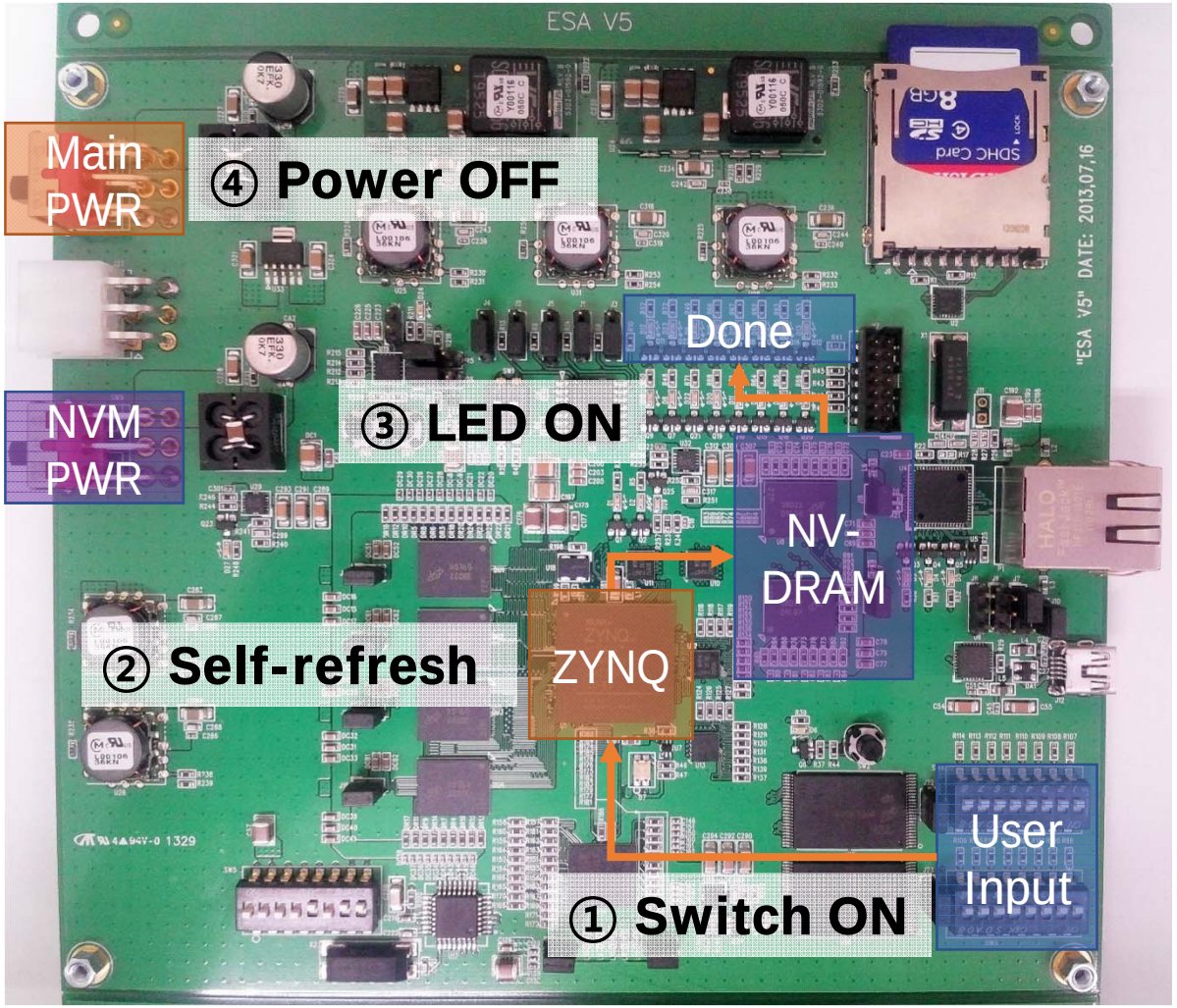
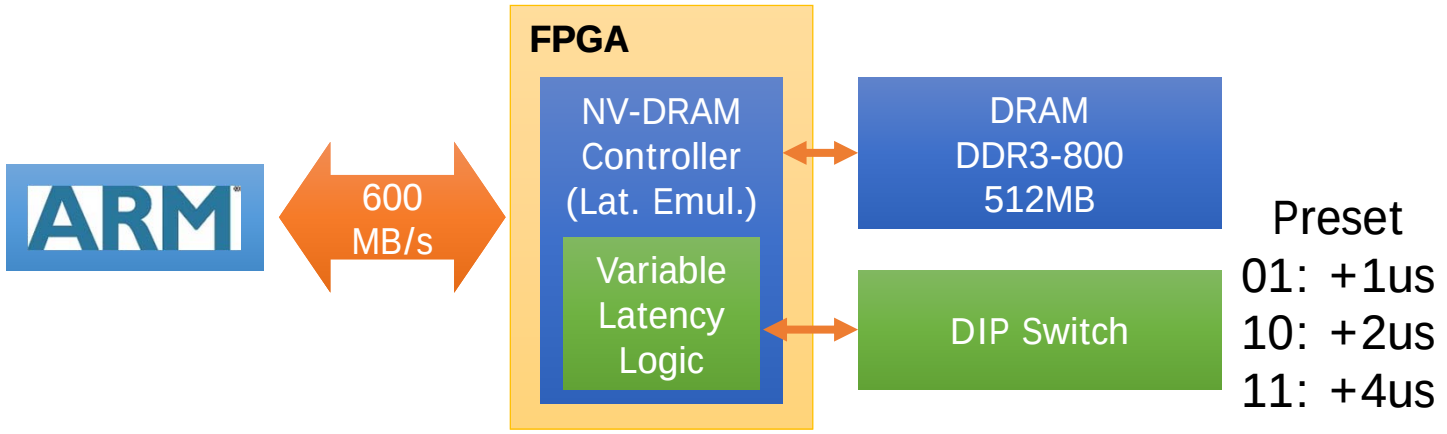


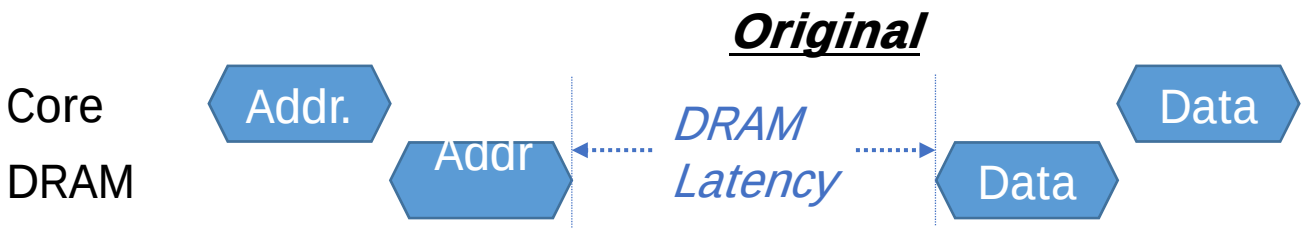
[Eom, NVRAMOS'12]

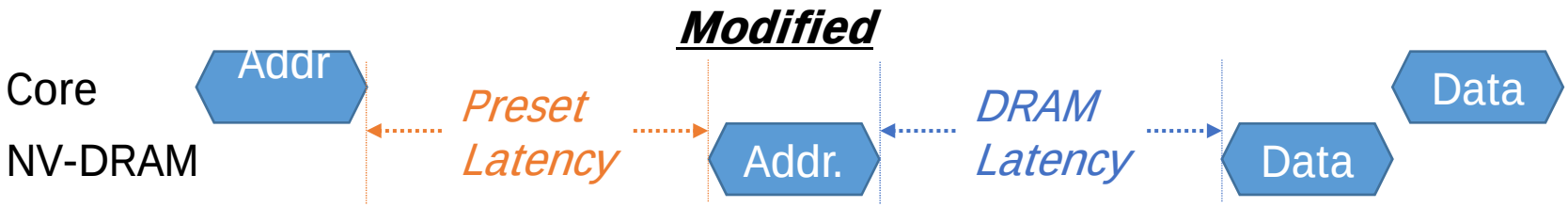
STT-RAM Emulation w/ DRAM



Latency Emulation (NV-DRAM)

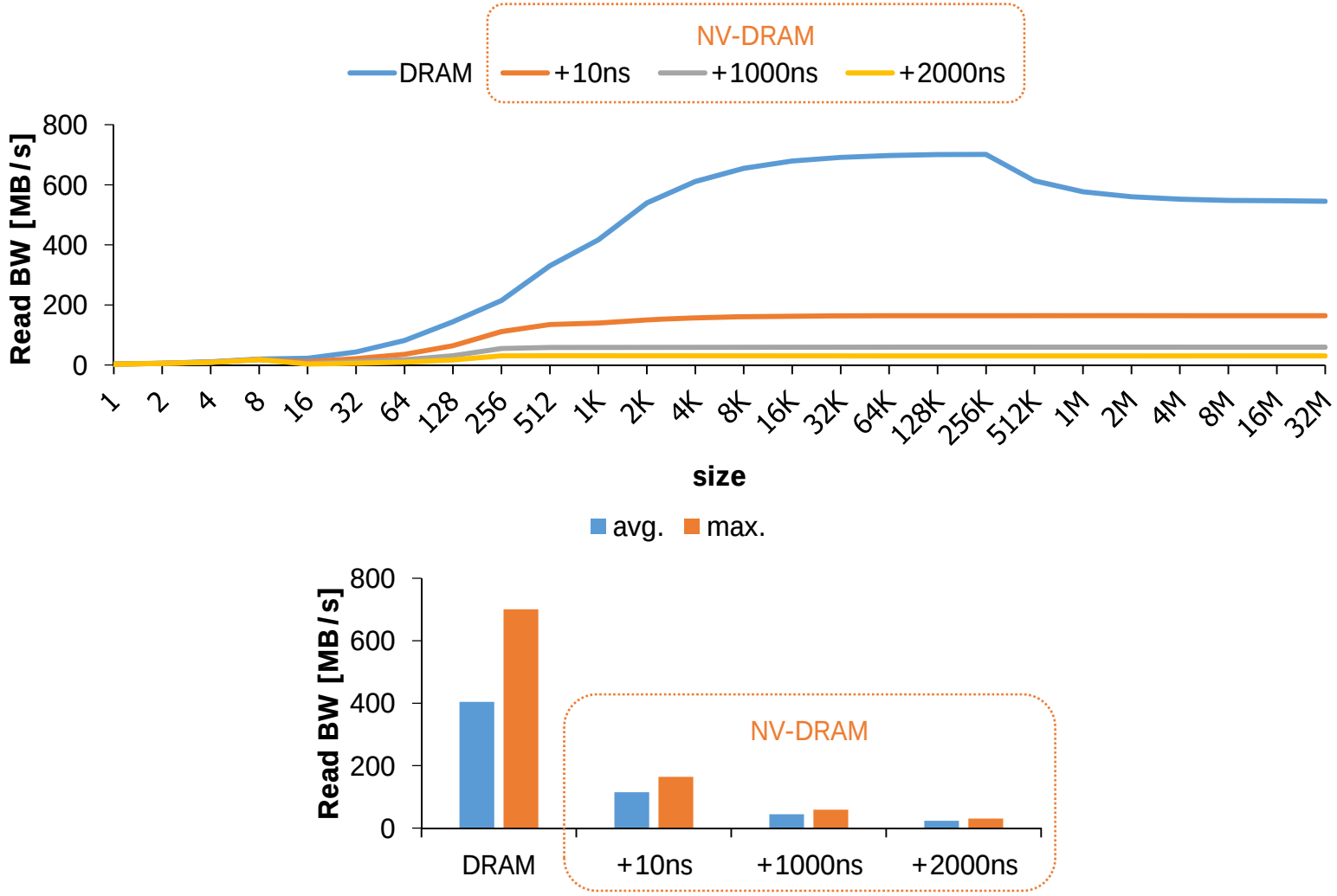




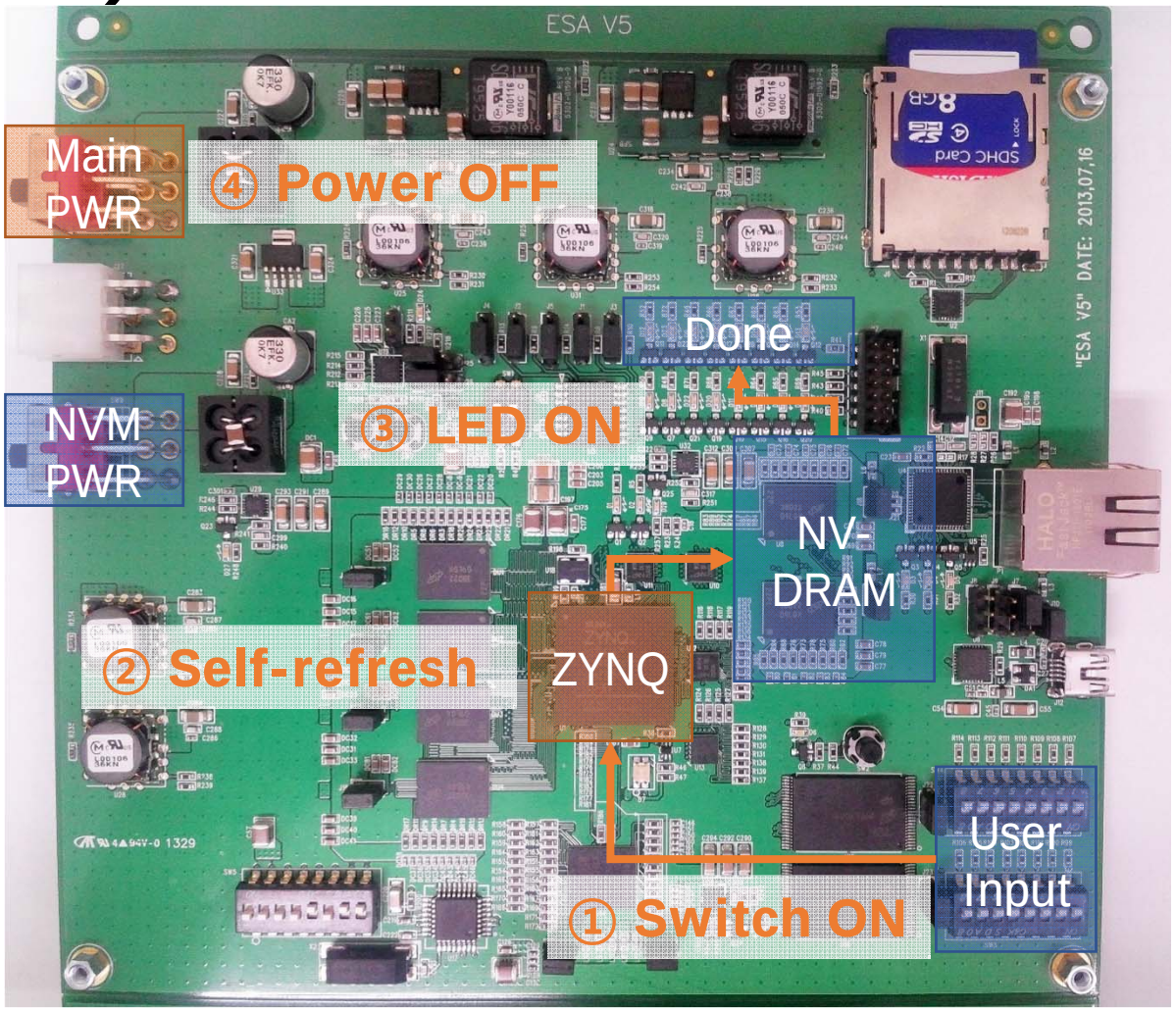


Read Bandwidth Sensitivity

BW = size / execution time of memcpy(size)



Non-Volatility Emulation (NV-DRAM)



Main Power OFF & NVM Power OFF

```
zynq-uboot> mw 0x40000000 0xaabbccdd 0x80
zynq-uboot> md 0x40000000 0x80
40000000: aabbccdd aabbccdd aabbccdd aabbccdd
40000010: aabbccdd aabbccdd aabbccdd aabbccdd
40000020: aabbccdd aabbccdd aabbccdd aabbccdd
40000030: aabbccdd aabbccdd aabbccdd aabbccdd
40000040: aabbccdd aabbccdd aabbccdd aabbccdd
40000050: aabbccdd aabbccdd aabbccdd aabbccdd
40000060: aabbccdd aabbccdd aabbccdd aabbccdd
40000070: aabbccdd aabbccdd aabbccdd aabbccdd
40000080: aabbccdd aabbccdd aabbccdd aabbccdd
40000090: aabbccdd aabbccdd aabbccdd aabbccdd
400000a0: aabbccdd aabbccdd aabbccdd aabbccdd
400000b0: aabbccdd aabbccdd aabbccdd aabbccdd
400000c0: aabbccdd aabbccdd aabbccdd aabbccdd
400000d0: aabbccdd aabbccdd aabbccdd aabbccdd
400000e0: aabbccdd aabbccdd aabbccdd aabbccdd
400000f0: aabbccdd aabbccdd aabbccdd aabbccdd
```

1min. later →

```
zynq-uboot> md 0x40000000 0x80
40000000: ab265780 d1d226a4 2e2a9a2c 55410174
40000010: 0808833e 554bc7c6 a090210a 59171400
40000020: 8a208804 15554149 2870a200 1352510a
40000030: 236ab298 04751507 82aae8bb 53fc1501
40000040: 20782a23 254a0059 2a8a0856 35415515
40000050: 29669428 e32765d6 983aa8b8 ec641449
40000060: b820828e 494bc494 e9201208 4308f5c1
40000070: a6ca8882 4d05314f 849a1e98 1d012164
40000080: aeab2822 855d4cd6 02a2bb08 5c4d4553
40000090: a2c1ae01 1e647415 8d824adc 53571145
400000a0: 2b388082 18da0415 c2022c98 00d15216
400000b0: b68a1821 47647209 a1f8f205 d4354141
400000c0: 622a289f 611dd9d4 a08a0860 54169171
400000d0: 682a9b98 117d4540 10b3ca2f 11d49408
400000e0: 8083a80c 14551886 02a8e306 10115547
400000f0: e0a210ac 12045555 868aa0a3 5c701455
```

Main Power OFF & NVM Power ON

```
zynq-uboot> mw 0x40000000 0xaabbccdd 0x80
zynq-uboot> md 0x40000000 0x80
40000000: aabbccdd aabbccdd aabbccdd aabbccdd
40000010: aabbccdd aabbccdd aabbccdd aabbccdd
40000020: aabbccdd aabbccdd aabbccdd aabbccdd
40000030: aabbccdd aabbccdd aabbccdd aabbccdd
40000040: aabbccdd aabbccdd aabbccdd aabbccdd
40000050: aabbccdd aabbccdd aabbccdd aabbccdd
40000060: aabbccdd aabbccdd aabbccdd aabbccdd
40000070: aabbccdd aabbccdd aabbccdd aabbccdd
40000080: aabbccdd aabbccdd aabbccdd aabbccdd
40000090: aabbccdd aabbccdd aabbccdd aabbccdd
400000a0: aabbccdd aabbccdd aabbccdd aabbccdd
400000b0: aabbccdd aabbccdd aabbccdd aabbccdd
400000c0: aabbccdd aabbccdd aabbccdd aabbccdd
400000d0: aabbccdd aabbccdd aabbccdd aabbccdd
400000e0: aabbccdd aabbccdd aabbccdd aabbccdd
400000f0: aabbccdd aabbccdd aabbccdd aabbccdd
```

1min. later →

```
zynq-uboot> md 0x40000000 0x80
40000000: aabbccdd aabbccdd aabbccdd aabbccdd
40000010: aabbccdd aabbccdd aabbccdd aabbccdd
40000020: aabbccdd aabbccdd aabbccdd aabbccdd
40000030: aabbccdd aabbccdd aabbccdd aabbccdd
40000040: aabbccdd aabbccdd aabbccdd aabbccdd
40000050: aabbccdd aabbccdd aabbccdd aabbccdd
40000060: aabbccdd aabbccdd aabbccdd aabbccdd
40000070: aabbccdd aabbccdd aabbccdd aabbccdd
40000080: aabbccdd aabbccdd aabbccdd aabbccdd
40000090: aabbccdd aabbccdd aabbccdd aabbccdd
400000a0: aabbccdd aabbccdd aabbccdd aabbccdd
400000b0: aabbccdd aabbccdd aabbccdd aabbccdd
400000c0: aabbccdd aabbccdd aabbccdd aabbccdd
400000d0: aabbccdd aabbccdd aabbccdd aabbccdd
400000e0: aabbccdd aabbccdd aabbccdd aabbccdd
400000f0: aabbccdd aabbccdd aabbccdd aabbccdd
```

Conclusion

- Prototyping system for new memory
  - Linux on ARM Cortex-A9
  - New memory controller design on FPGA
  - PRAM chip (LPDDR2-N)
  - STT-RAM emulation with DRAM
    - Additional latency and non-volatility
- On-going and future work
  - Large capacity in main memory
    - DDR3 DIMM for STT-RAM emulation
    - VA to PA translation schemes to reduce TLB misses
  - PRAM write performance improvement
    - Buffered write support
    - Multiple chips with better technology
      - Write bandwidth enhancement, e.g., 130MB/s [ISSCC'12]