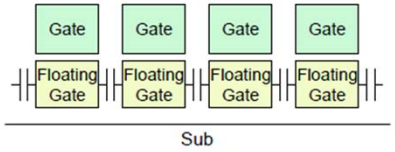
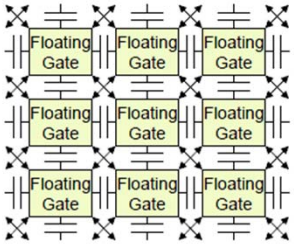
NVRAMOS 2013

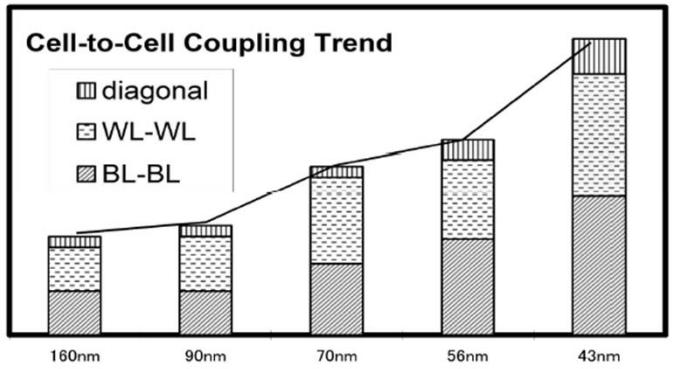
Data Corruption in even/odd bit-line Nand architecture

Cell to Cell Coupling





- Three components of CCC:
  - Diagonal
  - WL – WL
  - BL – BL
- CCC greatly affects final distribution width.
- With technology scaling, all 3 components of CCC increase.



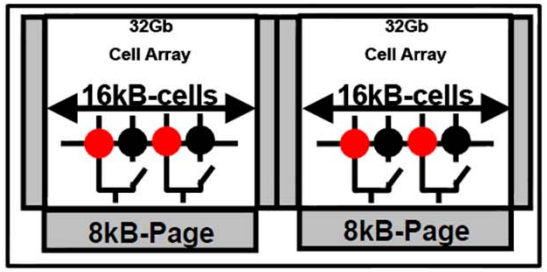
- With technology scaling, CCC increases dramatically
- To obtain tight distribution, need to overcome CCC

[source]
http://www.google.co.kr/url?sa=t&rct=j&q=&esrc=s&frm=1&source=web&cd=3&ved=0CEEQFjAC&url=http%3A%2F%2Fnvmw.ucsd.edu%2F2010%2Fdocuments%2FTrinh_Cuong.pdf&ei=dMFLUsrgB4uLkgWwk4G4Cw&usg=AFQjCNHUQrqSOEPoQc4OT9IiCFaDxnxurw&bvm=bv.53371865,d.dGI&cad=rjt

Even/Odd bit-line vs. ABL

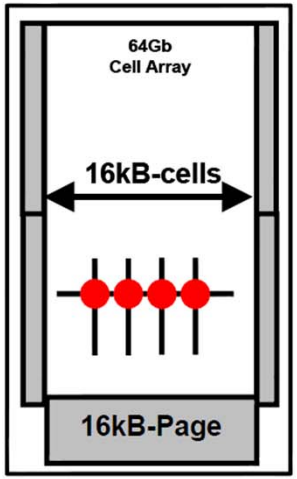
Single Array Configuration

Conventional
Evne / Odd Architecture



2-Plane array configuration

All-Bit-Line (ABL)
Architecture

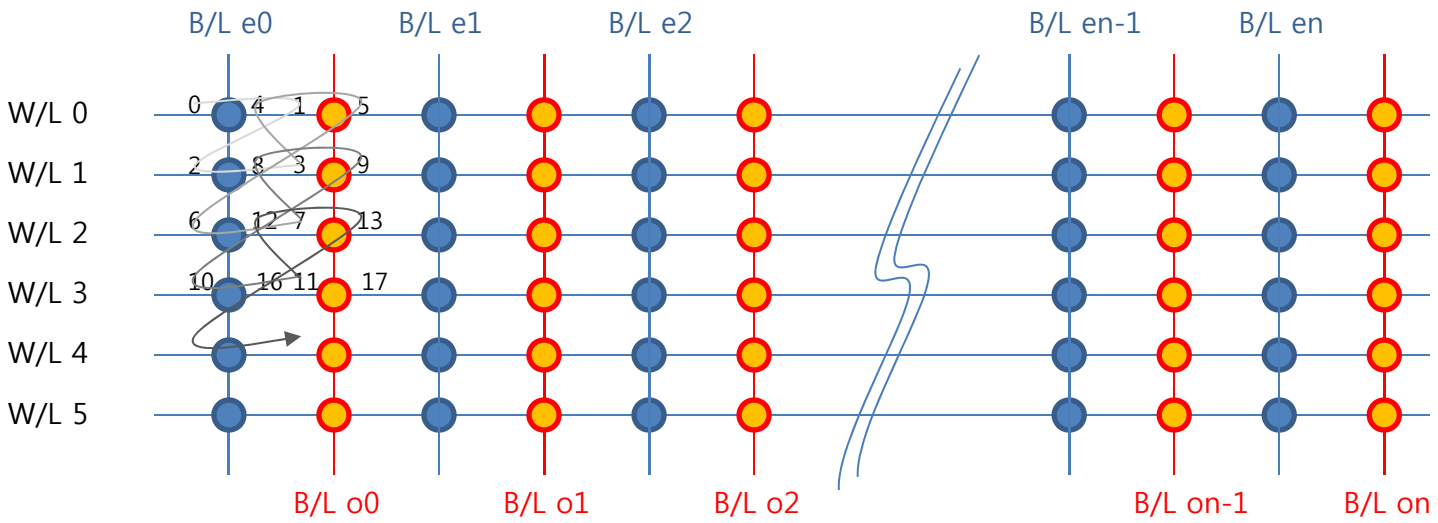


Single array configuration
⇒ Small Die size

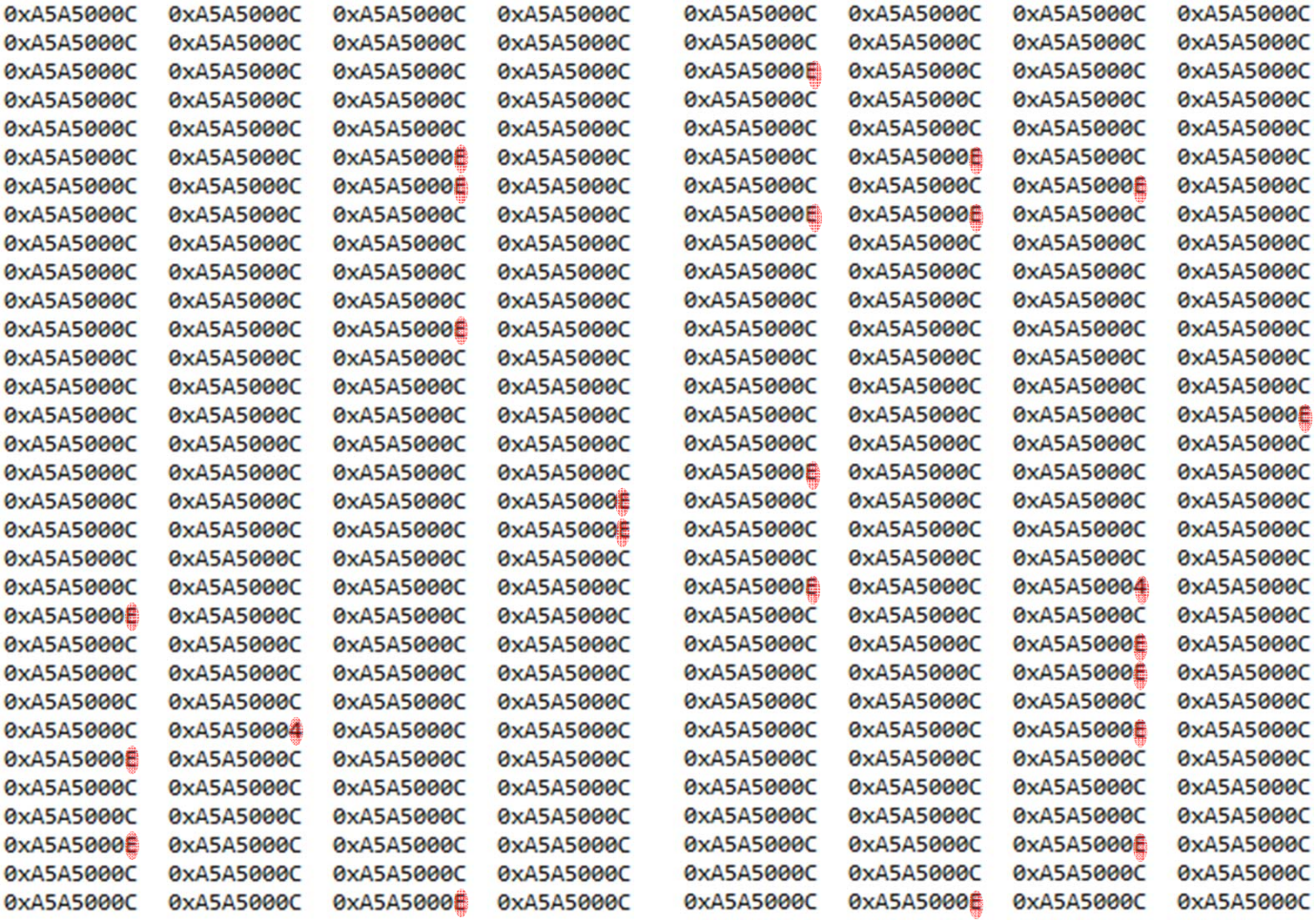
[source]
2012 flash memory summit TE21
19nm 112.8mm2 64Gb Multi-level Flash Memory with 400Mb/s/pin 1.8V Toggle Mode Interface

Paired Page Information
(conventional even/odd bit-line architecture)

	Paired Page address (Hex code)		Paired Page address (Hex code)	
	1st Group	2nd Group	1st Group	2nd Group
W/L 0	00	04	01	05
W/L 1	02	08	03	09
W/L 2	06	0C	07	0D
W/L 3	0A	10	0B	11
W/L 4	0E	14	0F	15
W/L 5	12	18	13	19



Even MSB page(#0x0C) corrupted data pattern



Even MSB page(#0x10) corrupted data pattern

0xA5A50010	0xA5A50018	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50012	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50018	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50012	0xA5A50010	0xA5A50010	0xA5A50010
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0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50012	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50018	0xA5A50012	0xA5A50010
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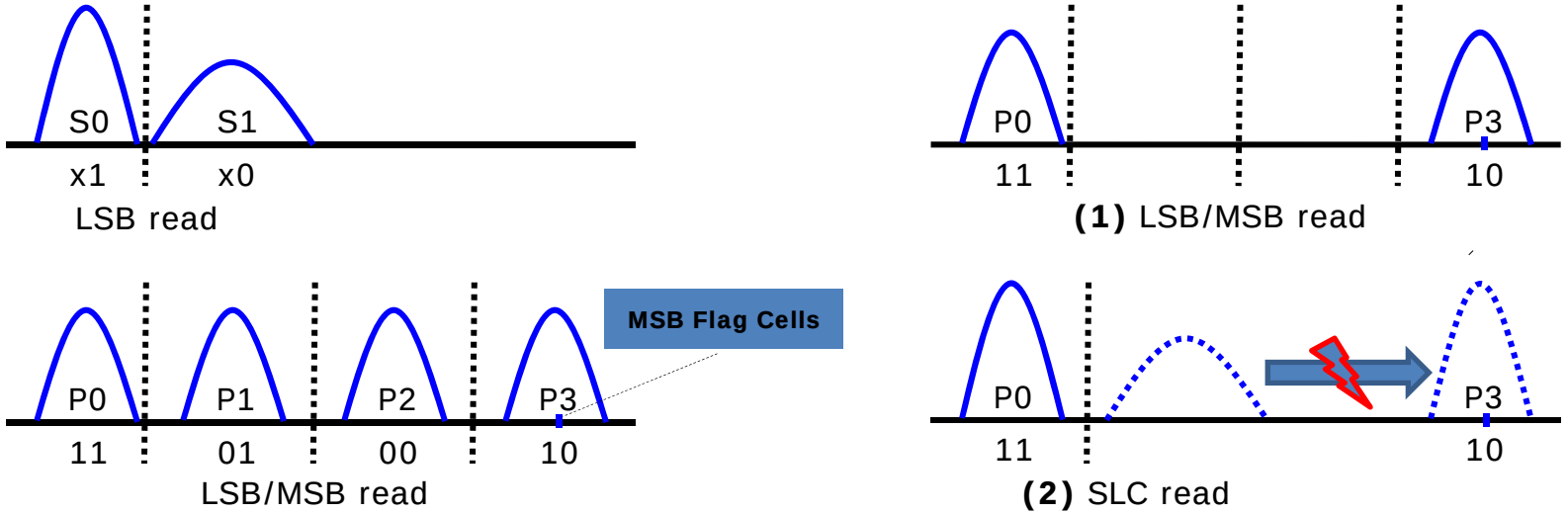
0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010	0xA5A50010
0xA5A50010	0xA5A50010	0xA5A50012	0xA5A50010	0xA5A50010	0xA5A50018	0xA5A50010	0xA5A50010

Higher reliability for LSB page data

paired LSB page corruption (MSB SPO)

Higher reliability for LSB page data of 2bit MLC NAND with the basic functions

- cell distribution
  - all cells' V_{th} distribution of the designated word line (X: V_{th} level, Y: cell count)
  - V_{th} : threshold voltage (voltage level to turn on floating gate)
  - world line : X-axis cell array, bit line : Y-axis cell array (a.k.a cell string)
- MLC programming scenario in the general terms
  - LSB page program makes two hills as the first program to the designated word line
  - MSB page program splits two hills into four hills and shifts each hill into the corresponding voltage range
- Key idea
  - Sudden power off or Power loss during MSB page program shall make LSB page data corrupted
  - To make LSB page data more reliable, (1) program all 1's into MSB page, (2) SLC read from LSB page if it would show uncorrectable ECC error through MLC read
- Benefits
  - Whole blocks can be handled as MLC block → no needs for SLC blocks, simpler block management, et cetera