

# Leading Next Storage era Through Vertical Optimization

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TheAIO Co., Ltd.

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# Company Overview

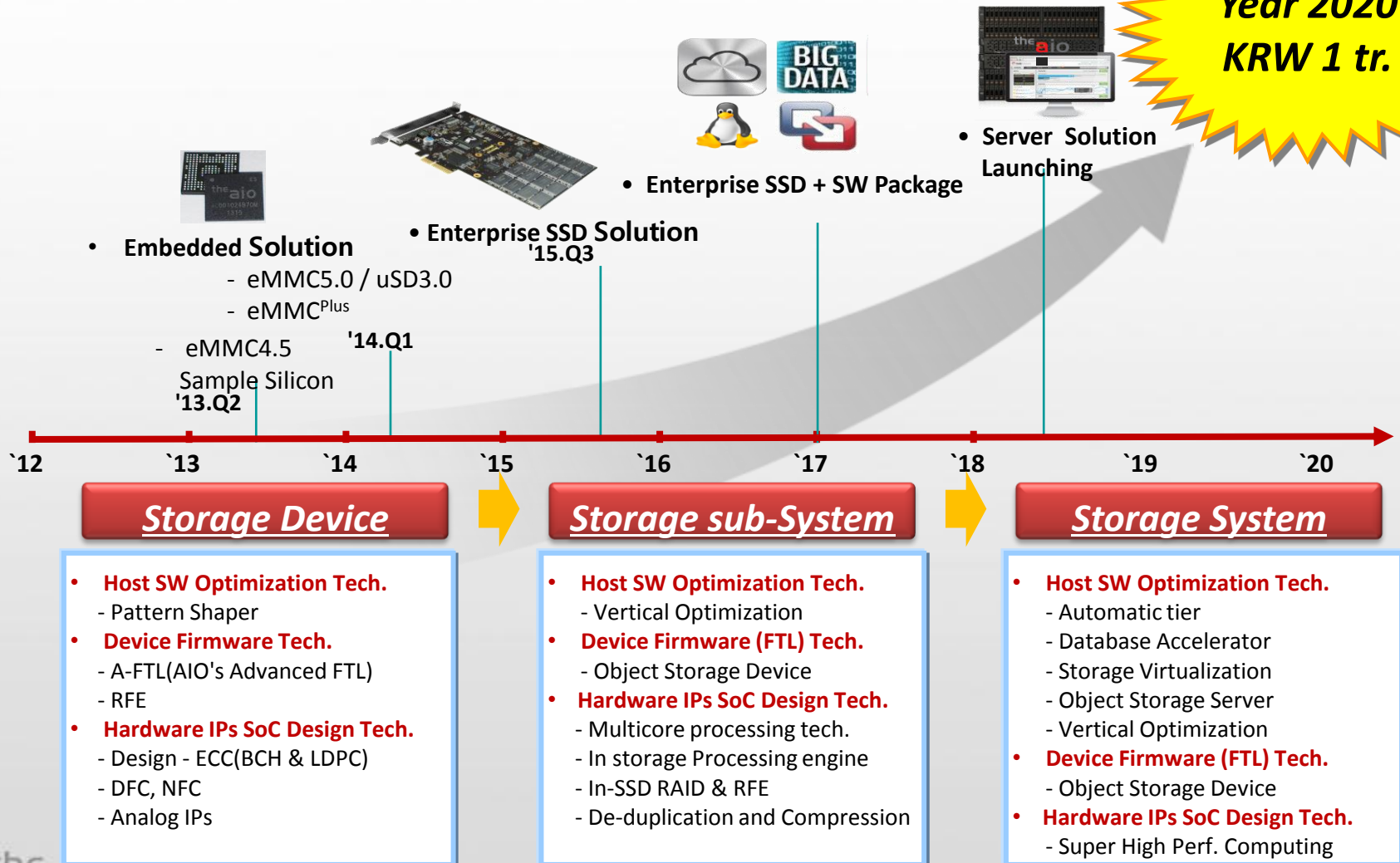
|               |   |
|---------------|---|
| Company Name  | The-AIO / the-aio co., Ltd. (The Advanced IO)   |
| Vision        | Total Storage Solution Provider   |
| Establish Day | Jun 16 <sup>th</sup> 2011   |
| CEO           | Jin-Hyoung, Kwon ( <a href="mailto:jh.kwon@the-aio.com">jh.kwon@the-aio.com</a> )   |
| Products      | <ul style="list-style-type: none"> <li>• Standard Product : eMMC/UFS/SD controller and S/W</li> <li>• Differentiated Product : SpikeNAND™, eMMC<sup>plus</sup> etc. controller and S/W</li> <li>• Storage Sub-System : Enterprise SSD + SW Package</li> </ul> |
| Members       | 49 People (R&D proportion <b>84%</b> )  |
| Address       | KINS Tower 17 <sup>th</sup> Floor, 25-1, Jeongja-dong, Bundang-gu<br>Sungnam-si, Gyeonggi-do, Korea   |
| Contact       | Tel : +82-31-716-0170<br>Fax : +82-31-716-0580<br>E-Mail : Sales@the-AIO.com<br>Home Page : <a href="http://www.the-AIO.com">www.the-AIO.com</a>  |



# Vision

## Total Storage Solution Provider

**Year 2020  
KRW 1 tr.**

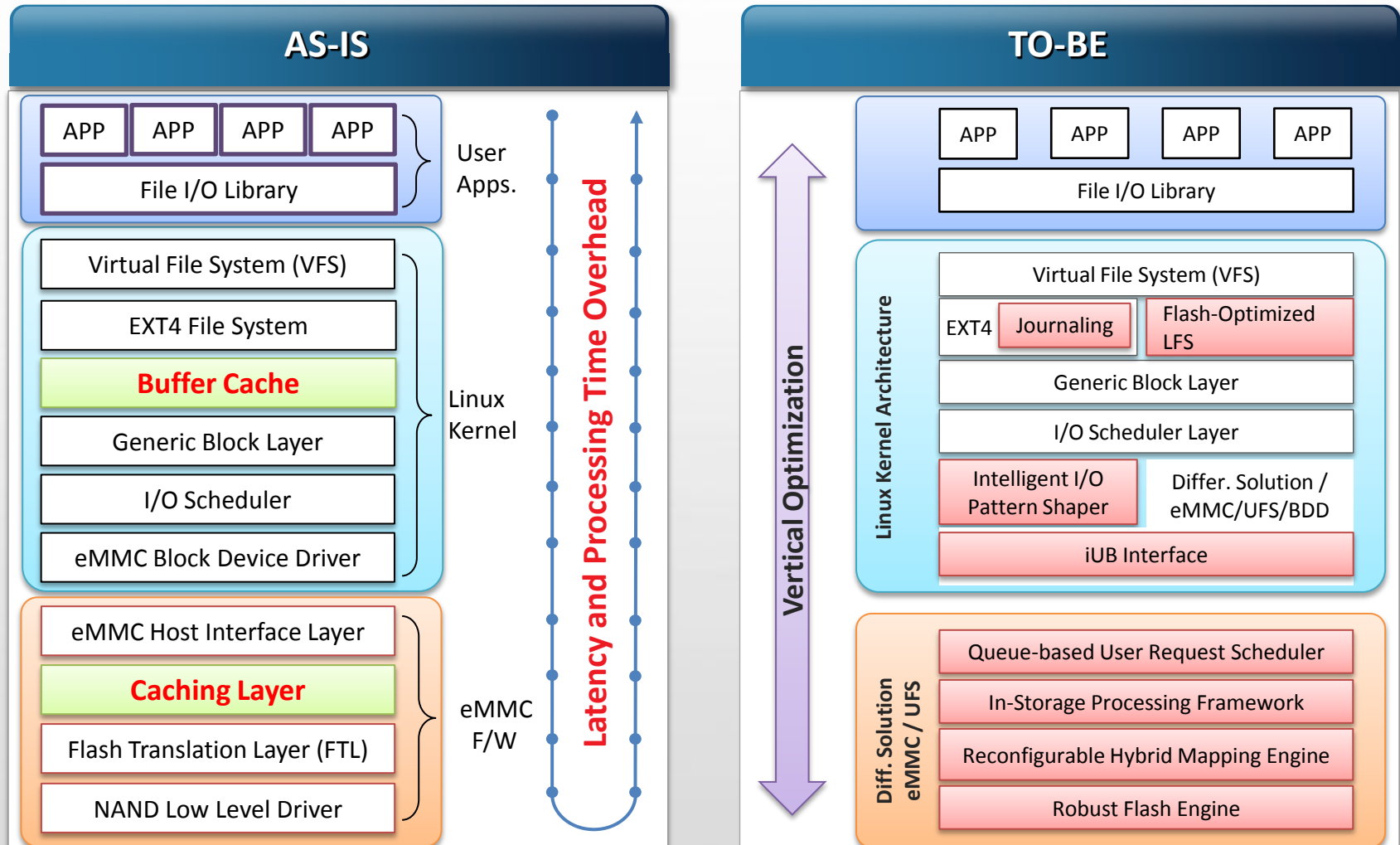




## Vertical Optimization and Integration

# Key Technology for Next Storage Era

- Legacy storage stack which was developed for HDD has many limitation



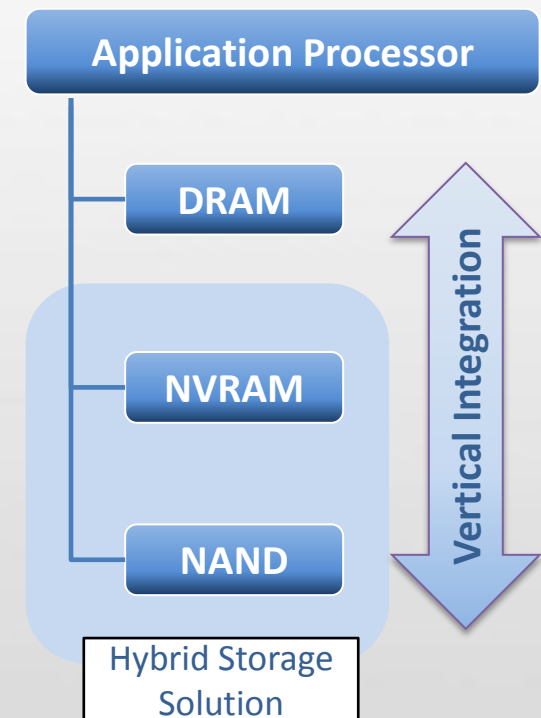
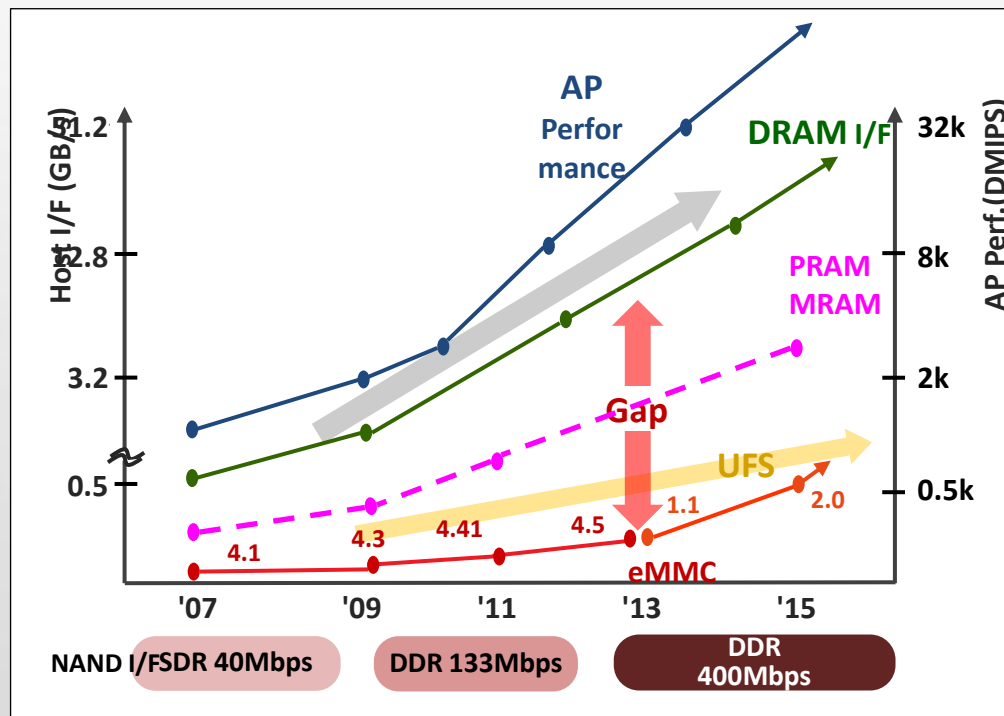
# Needs for better storage performance

## ■ NVRAM can be a new solution for better storage performance

- Pros.: NVRAM can compensate for the performance gap between DRAM and NAND
- Cons.: Need to clear issues from marketability and capacity

## ■ AIO is proposing a NVRAM-NAND hybrid storage solution

- NVRAM-NAND hybrid storage solution covers NVRAM standalone issues

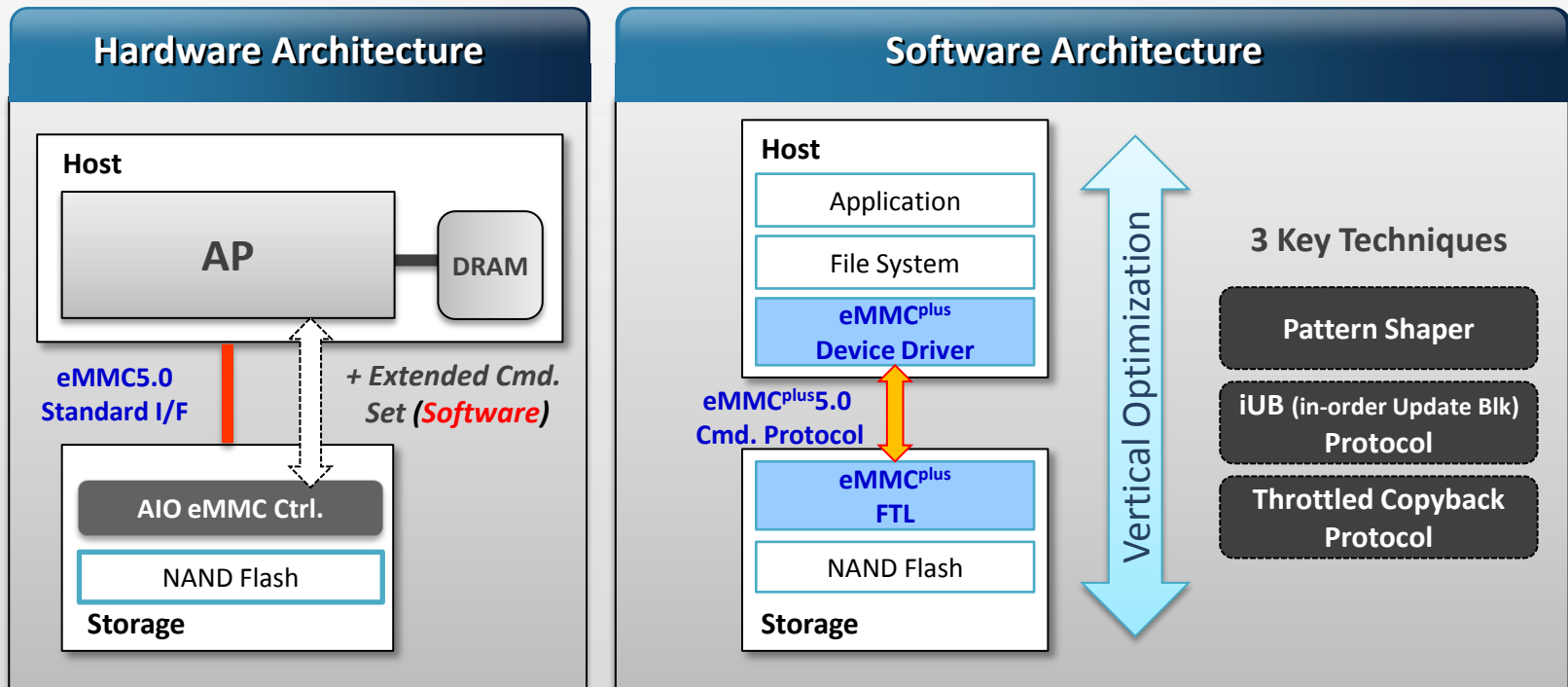




**Current optimized solution**

# eMMC<sup>plus</sup> 5.0 Solution

- Advanced eMMC Solution with Full Compatibility with Standard eMMC5.0
  - No Host Side HW Change needed
- Higher Performance
  - **10x Higher Random Write Performance** : Pattern Shaper
- Reliability with Low Cost TLC NAND
  - **4x Longer Endurance** : Pattern Shaper / iUB → **Low Cost (TLC instead of MLC)**





# Demo: Competitor eMMC vs. eMMC<sup>plus</sup>

## Androbench Settings

- Write file-size : 16MB
- Read file-size : 32MB
- Sequential IO size : 256KB
- Random I/O size : 4KB
- # of SQL transaction : 1000

## File system utilization: 0%

## NAND : 64Gb MLC x 2 way



|                  | Competitor       | AIO eMMC <sup>plus</sup> |
|------------------|------------------|--------------------------|
| Sequential Read  | 93.2 MB/s - 5.7% | 87.8 MB/s                |
| Sequential Write | 22.6 MB/s 26.4%  | 28.5 MB/s                |
| Random Read      | 12.9 MB/s 23.0%  | 15.9 MB/s                |
| Random Write     | 1.5 MB/s 69.5%   | 2.5 MB/s                 |
| SQLite Insert    | 112.4 TPS 25.4%  | 140.9 TPS                |
| SQLite Update    | 113.7 TPS 8.0%   | 122.8 TPS                |
| SQLite Delete    | 120.7 TPS 11.7%  | 134.8 TPS                |
| Browser          | 54.3 ms 57.0%    | 34.6 ms                  |
| Market           | 128.9 ms 12.6%   | 114.5 ms                 |
| Camera           | 121.9 ms 15.1%   | 105.8 ms                 |
| Camcorder        | 266.2 ms 6.8%    | 249.2 ms                 |
| Total Time       | 72"              | 47"                      |

# eMMC<sup>plus</sup> 4.51: Performance Summary

■ MP version silicon is expected to *outperform competitors by significant amount*

[ Performance in OS-less environment (over raw device) ]

| OS-Less<br>(Raw Device) |         | 1 <sup>st</sup> Silicon |                      | MP Silicon (Estimated) |                      | eMMC 4.51 Competitor |          |          |
|-------------------------|---------|-------------------------|----------------------|------------------------|----------------------|----------------------|----------|----------|
|                         |         | 1Ch. 2way 16GB@DDR200   |                      | 1Ch. 2way 16GB@DDR266  |                      | 1x2 16GB             | 1x2 16GB | 1x4 16GB |
|                         |         | eMMC                    | eMMC <sup>plus</sup> | eMMC                   | eMMC <sup>plus</sup> | A                    | B        | C        |
| Sequential<br>(MB/s)    | Read    | 140                     | ←                    | 180                    | ←                    | 169                  | 166      | 125      |
|                         | Write   | 62                      | ←                    | 80                     | ←                    | 37                   | 60       | 38       |
| Random<br>(IOPS)        | S-Read  | 8,774                   | ←                    | 9,000                  | ← <sup>†</sup>       | 7,501                | 5,450    | 4,553    |
|                         | A-Write | 3,011                   | 15,872               | 3,100                  | 17,920               | 2,110                | 2,388    | 2,243    |

[ Performance in Android-Linux environment (over file system, AIOzone) ]

|                      |         |       |        |                    |                    |       |       |       |
|----------------------|---------|-------|--------|--------------------|--------------------|-------|-------|-------|
| Sequential<br>(MB/s) | Read    | 111   | 116    | 120                | 120                | 102   | 99    | 83    |
|                      | Write   | 58    | 61     | 70                 | 70                 | 34    | 47    | 35    |
| Random<br>(IOPS)     | S-Read  | 3,316 | 3,073  | 3,400              | 3,400 <sup>†</sup> | 2,949 | 2,648 | 2,278 |
|                      | A-Write | 1,819 | 11,666 | 2,000 <sup>‡</sup> | 13,200             | 1,737 | 1,575 | 1,356 |

Note1: eMMC<sup>plus</sup> performance is calculated based on eMMC performance

Note2: NAND for AIO eMMC – 64Gb MLC of B company (1xnm)

† Constant regardless of range (iUB mapping)

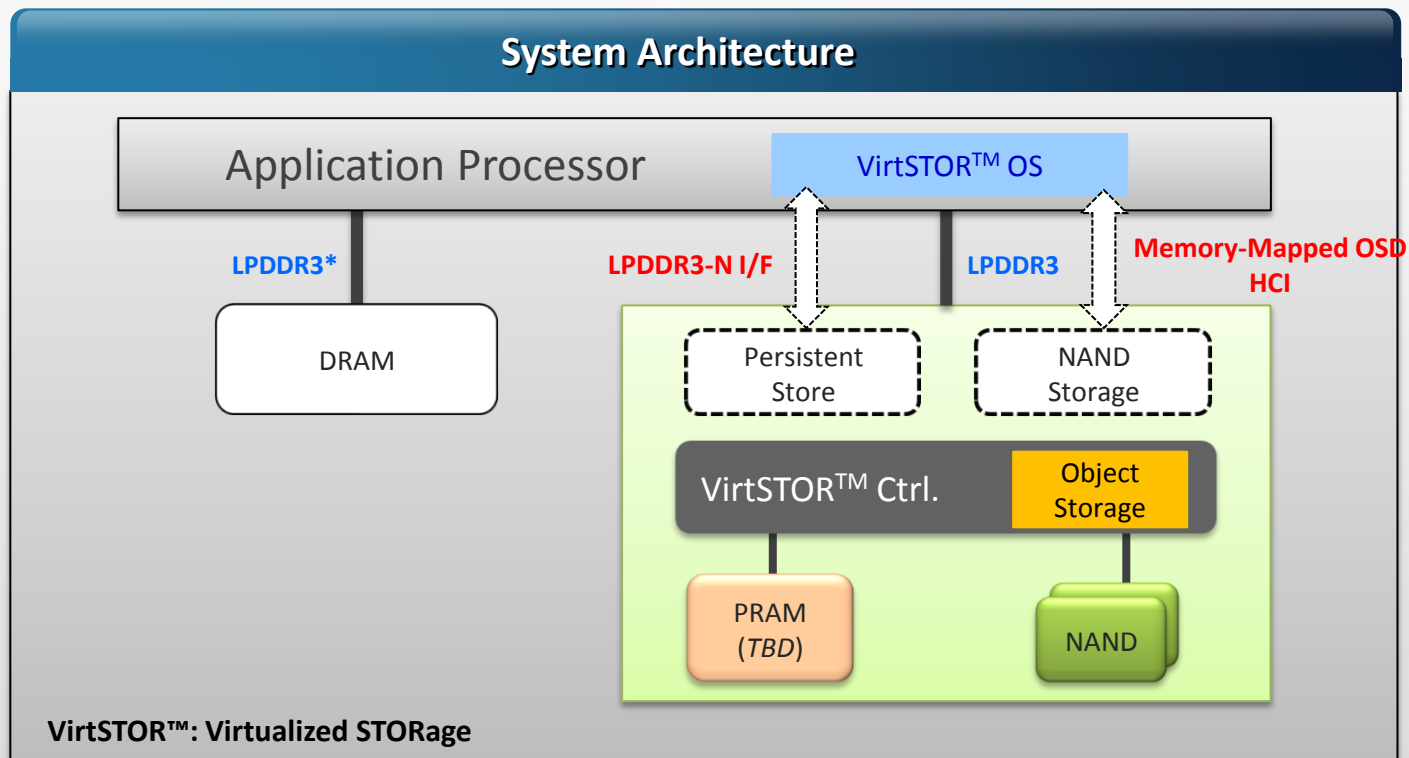
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**Preparing the new NVRAM era**

# VirtSTOR™: NVM-Powered Storage Solution

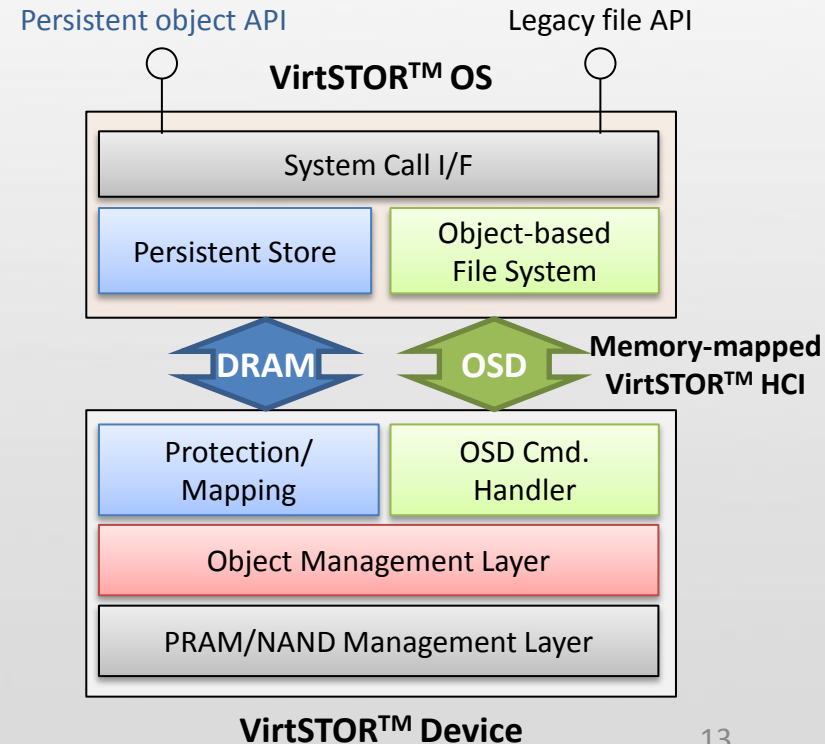
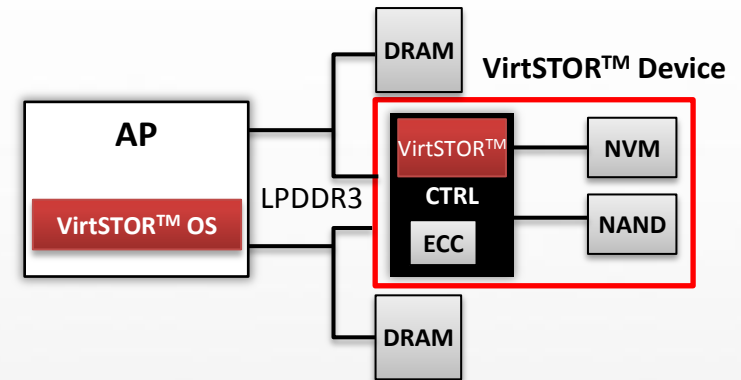
- NVM-Unified Solution to Improve Performance and Reliability
  - NVM-Powered : **Ultra Fast Random Performance, Reliability Enhancement**
  - Dual-Mode Access : Persistent Object Interface, Object-Storage Device (OSD) Interface
  - Object-based NAND Space Management : Common Backend Store



\* Could be LPDDR3/4 or other next generation DRAM interface (TBD)

# VirtSTOR™ Technology

- **Object-based NAND space management**
  - Common backend store
  - Infrastructure for intelligent storage; i.e., In-storage Processing Engine
- **Tiered storage with NVM at the first tier**
  - Un-buffered small random writes
    - E.g., Database, journal data, lock files, meta data of file system and FTL
  - Temporary data update
    - E.g., LSB/CSB backups
- **Internal use of NVM**
  - FTL meta management
  - NAND reliability information storage
- **Thin-provisioning of NVM**
  - Swapping between PRAM ↔ NAND
- **Hardware-assisted PRAM access**
  - TLB for minimum access latency
  - Protection mechanism



# Effectiveness of Proposed Architecture

## High Performance

- NVRAM absorbs random write traffic from applications and file systems
- Application directly accesses persistent store; no OS overhead
- Fast booting and application start-up; recovery but no reconstruction, XIP

## High Reliability and Endurance

- Smaller WAF(write amplification Factor); random writes to NVRAM
- In-storage RAID technique; NVRAM as a parity store
- LSB/CSB page data backup and NAND reliability information in NVRAM

## Easy integration and Maintenance

- Thin file system stack in operating system
- Tiering is performed autonomously by storage
- Architecture transparent to application and file system

## Low Cost

- Thin provisioning of NVRAM with high capacity backup storage (i.e., NAND)
- Smaller SRAM usage for NAND management

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## **Conclusion**

# New Storage Solution Era begins with Cooperation

**NVRAM Development**

*Memory  
Vendors*

**Storage Solution**

*Solution Vendor* the **aio**

*Next Gen.  
Storage  
Eco-System*

*Academies*

*Set Makers*

**Arch. Exploration &  
Concept Validation**

**Integration &  
Commercialization**



# Thank You

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