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Reduced-DRAM Architecture for Enterprise SSDs: Trends, Challenges, and How We Tackle Them

2026

Product Planning Lead
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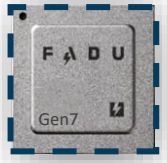
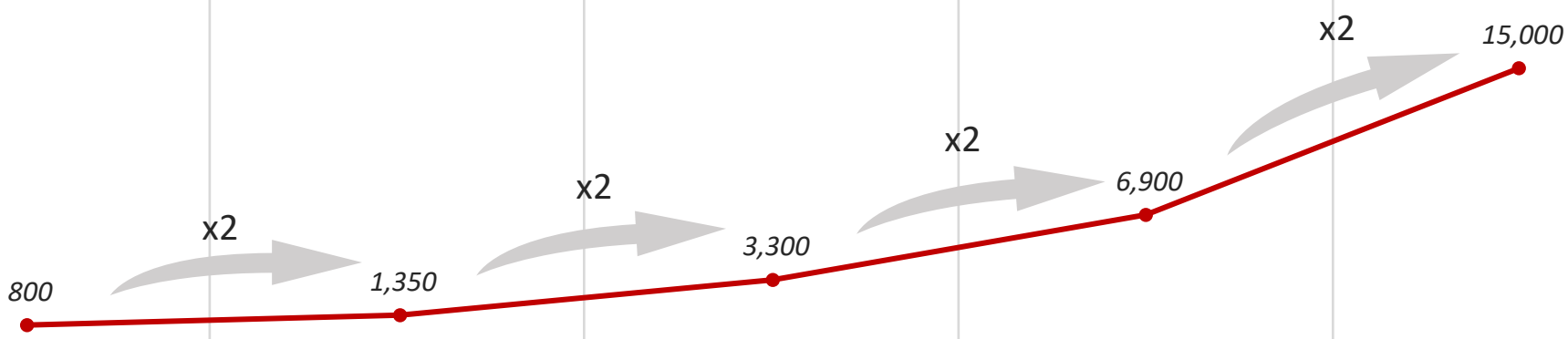
Product Line-up

- Proven track record : Controller development to mass production with no full layer revision
- Gen6 development (Controller + FW) is on-track
- Gen7 market and customer requirements under review, along with development feasibility assessment

	Jul. 2018~ PCIe Gen3 x4	Aug. 2020~ PCIe Gen4 x4	Nov. 2022~ PCIe Gen5 x4	2Q 2026~ PCIe Gen6 x4	2028~ PCIe Gen7 x4
Controller	 FC3081 NVMe 1.4 / 8ch	 FC4121 NVMe 1.4 / 12ch	 FC5161 NVMe 2.0 / 16ch	 FC6161 (Lhotse) NVMe 2.3 / 16ch	 FC7161 (Makalu) NVMe 2.4 / 16ch (TBD)
Performance **Ran. Read (kIOPs)**					

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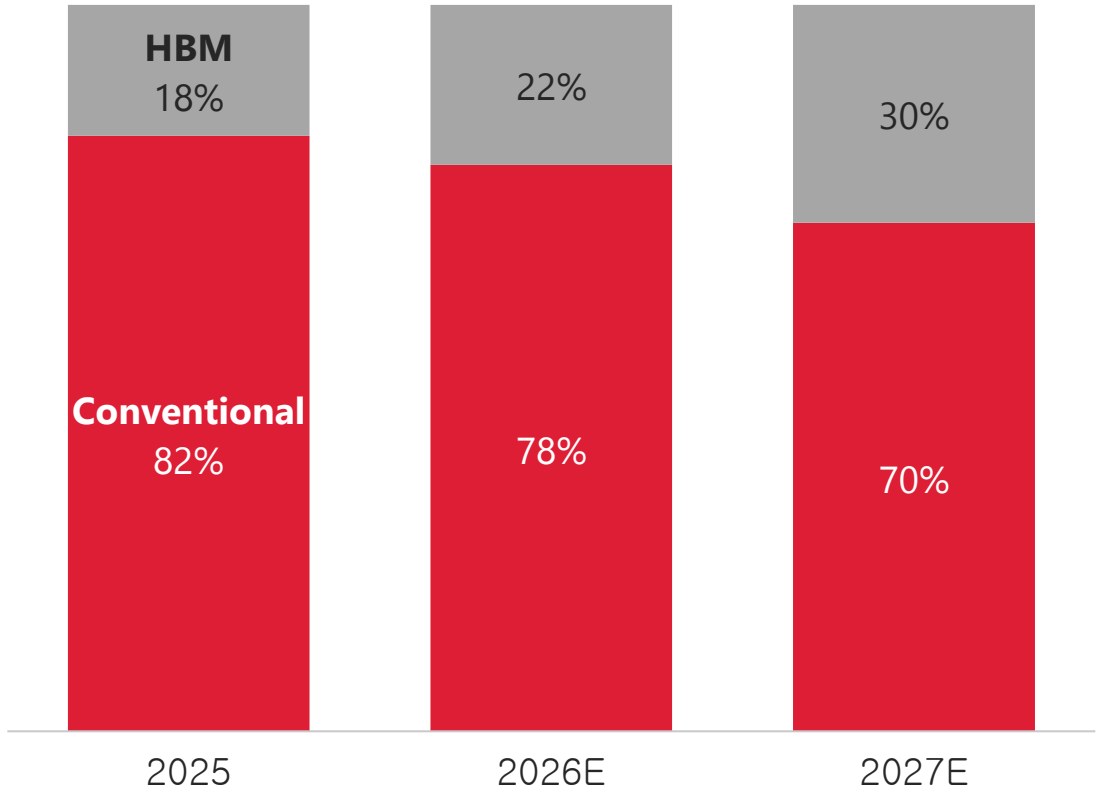
Trend (1/4) – HBM Takes Wafers from SSD DRAM

DRAM wafer input by product, top-3 suppliers, % (year-end)



- **HBM takes ~30% of wafers, returns ~13% of bits**
  - ✓ Top-3 HBM wafer input: 18% → 22% → ~30% (2025–2027)[1]
  - ✓ HBM bit share, same period: 8% → 9% → ~13%[1]
- **One HBM die uses ~3x the wafer area of DDR5**
  - ✓ Each +1%p of HBM wafer share removes 2–3x as many conventional bits[2]
  - ✓ Samsung (Sep 2026): HBM ~20% of industry wafers now, nearly 30% in 2027[2]
- **eSSD DRAM (DDR5/LPDDR5X) comes from the conventional share, down from ~82% to ~70% by 2027**

Conventional = DDR5, LPDDR5X, GDDR and legacy DRAM; no public wafer split by type. [1]TrendForce (Jun 2026). [2]Reuters, Samsung EVP Kim Taewoo (Sep 2026).

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Trend (2/4) – SSDs Get DRAM Last, After AI Servers

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Why suppliers serve servers first

Indicator	Value
Supply: servers take the bits	
HBM + server RDIMM share of DRAM bits, 2026E	**51%**
Server RDIMMs that are DDR5, 2Q26 (excl. HBM; same die as eSSD DRAM)	**>90%**
Demand: AI drives the growth	
AI share of DRAM demand, 2025 → 2026E	**16% → 26%**
Price: servers pay the most	
Server share of DRAM revenue, 2Q26	**~49%**
Server DRAM contract price, 2026E vs. 2025	**~+270%**

Allocation order for incremental DRAM bits

1 **HBM**
AI accelerators (GPU, ASIC)

2 **Server RDIMM / SOCAMM**
LTA customers: CSPs, server OEMs

3 **Non-LTA server volume**
Spot and incremental orders

4 **PC, mobile, SSD / embedded**
Remaining bits, highest price

- From 3Q26, price hikes hit non-LTA buyers first[1]
- 2027 RDIMM supply: +15–20% YoY, below server CPU growth[1]
- **SSD vendors buy outside LTAs: last in line on price and volume**

[1]TrendForce quarterly DRAM price and revenue reports (2Q26–4Q26). Server DRAM excludes HBM per TrendForce definition (to be confirmed). Baird memory sector research (2026): AI-linked demand share.

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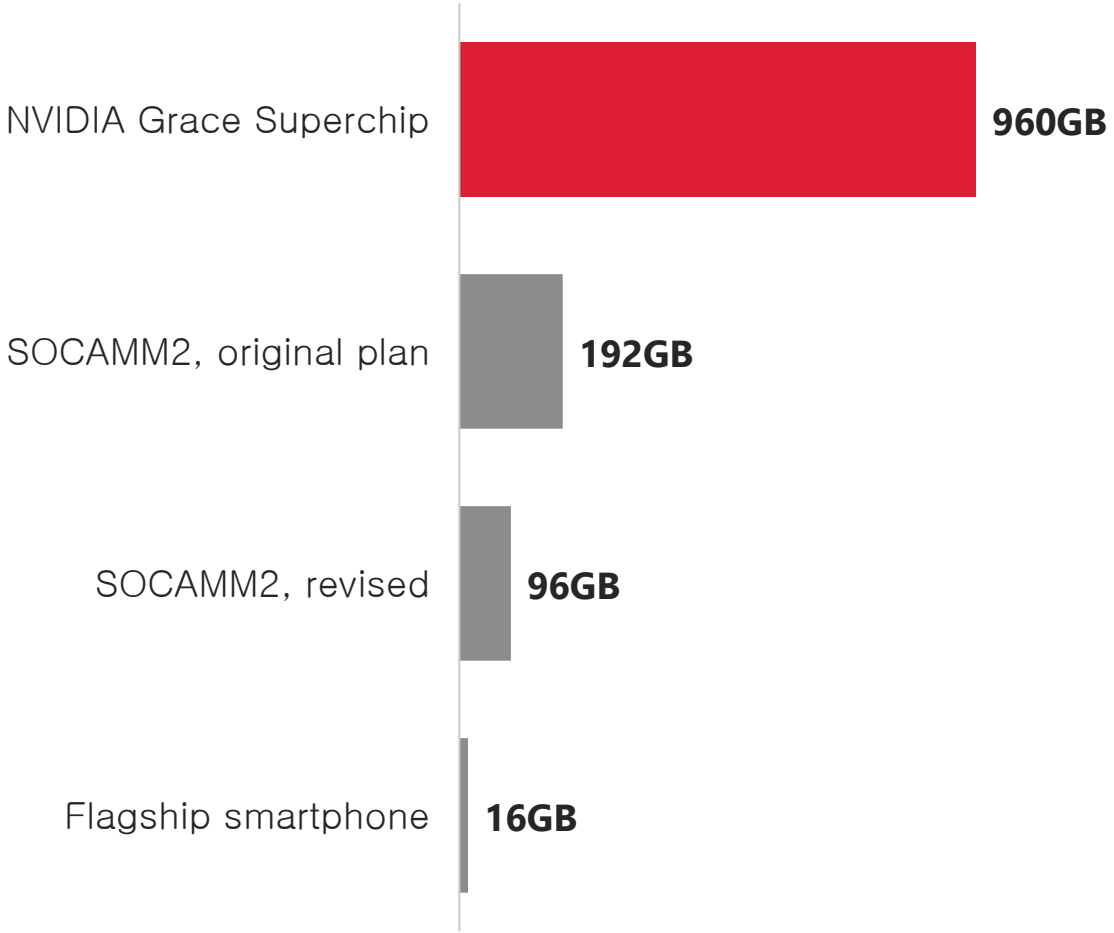
Trend (3/4) – AI Servers Absorb LPDDR5X Supply

LPDDR5X content per unit, GB



- **AI servers now buy LPDDR5X at smartphone-OEM scale**
  - ✓ NVIDIA Grace: up to 960GB per superchip, 60x a 16GB flagship phone
  - ✓ Counterpoint: the LPDDR shift makes NVIDIA a customer the size of a major phone maker[2]
- **Even NVIDIA cannot get enough**
  - ✓ SOCAMM2 capacity cut from 192GB to 96GB on LPDDR shortage (Jun 2026)[2]
  - ✓ AI data center LPDDR5X demand keeps growing through 2026 into 2027[2]
- **LPDDR5X contract price +78–83% QoQ in 2Q26**[1]
  - ✓ Flagship phones step down from 16GB to 12GB; mid-range back to 8GB[1]
- **Servers take LPDDR5X; PC, mobile and SSD get pushed out**

AI PCs also add on-package LPDDR5X per unit, but servers (Grace, SOCAMM) drive the shortage.
[1]TrendForce mobile DRAM contract price survey (May 2026). [2]Counterpoint Research; The Elec (Jun 2026); DigiTimes (5 Oct 2026); NVIDIA Grace CPU Superchip spec.

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Trend (4/4) – DRAM Stays Short Until 2028

(a) Supplier inventory

<10 days

Samsung + SK hynix DRAM, Sep 2026[1]

30–45 days

Normal level[1]

(b) DRAM supply outlook by year

Year	Supply status
2026	Supply short of demand: sufficiency ratio −1% to −2%[2]
2027	Gap widens; SK hynix expects the tightest year[3]
2028	Still tight (Samsung[4], Micron[5]); SK hynix M17 opens in Dec
2029	SK hynix Yongin Y2 first clean room in Jun
2030+	Demand still above supply[3]

(c) 2026 DRAM capex by supplier

Supplier	2026 DRAM capex[6]	Main use
Samsung	~$20.0B	HBM on 1c node; small P4L expansion
SK hynix	~$20.5B	M15X fab for HBM4
Micron	~$13.5B	1-gamma node migration, TSV tools
Industry	$53.7B → $61.3B (+14%)	Node upgrades, high stacking, hybrid bonding, HBM

New capex goes to HBM and node migration; clean-room limits keep conventional bit growth low until 2028[6]

[1]KB Securities via Seoul Economic Daily (7 Sep 2026). [2]TrendForce DRAM sufficiency outlook (2026). [3]SK hynix CEO remarks (2026). [4]Samsung 2Q26 earnings call (30 Jul 2026). [5]Reuters on Micron (30 Sep 2026). [6]TrendForce DRAM capex report (13 Nov 2025).

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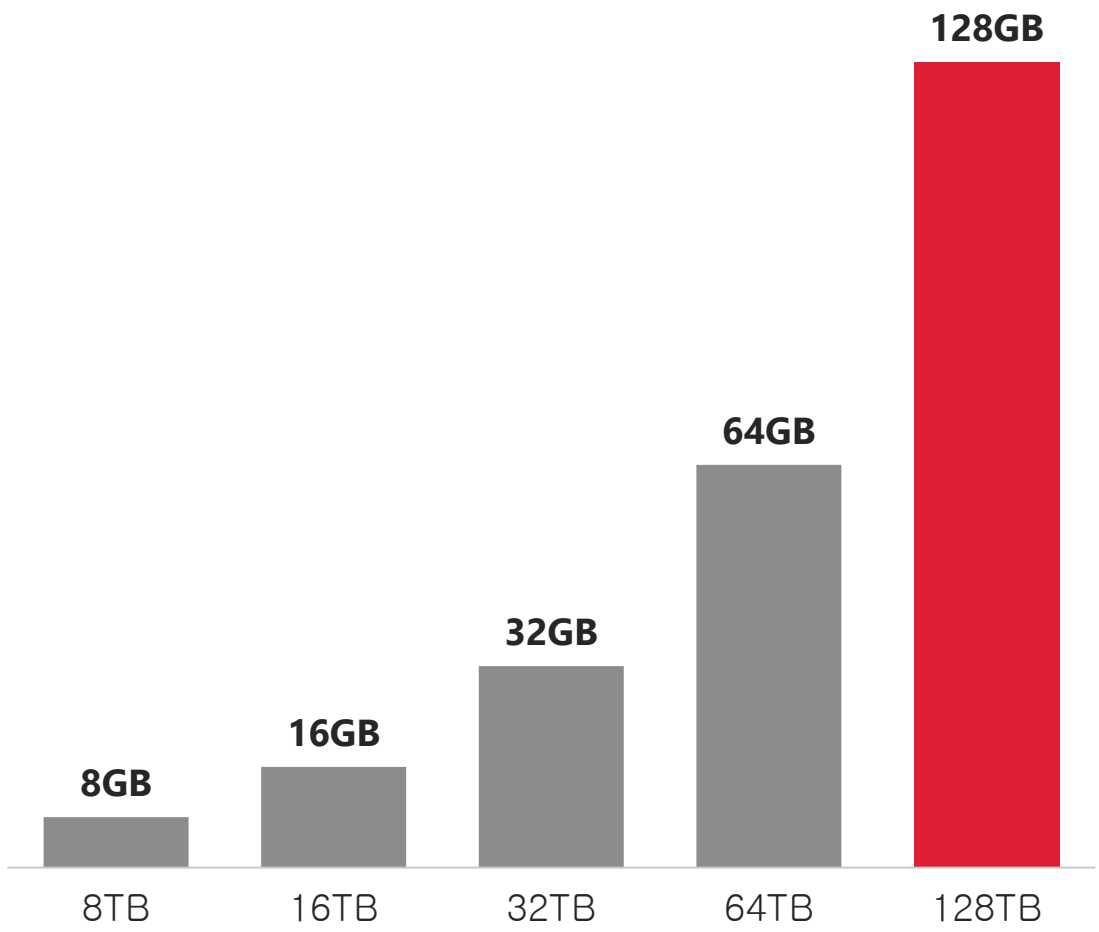
Impact (1/2) – eSSD DRAM Grows 1GB per TB of NAND

DRAM per eSSD with full L2P map, by NAND capacity



- **Full L2P map: ~1GB of DRAM per 1TB of NAND**
  - ✓ 16TB needs 16GB; 128TB needs 128GB, one server RDIMM
- **DDR5 now costs ~6x more than a year ago**
  - ✓ DDR5 16Gb spot ~$60 per chip (Oct 2026), +480% YoY[2]
  - ✓ Contract price +90–95% QoQ in 1Q26, +58–63% in 2Q26[1]
- **No LTA, so SSD vendors pay the highest price**
  - ✓ Same buyer position as PC and mobile OEMs: non-LTA price, last allocation
  - ✓ LTAs signed from 2Q26 carry price ceilings; non-LTA buyers take the hikes[3]

Reduced DRAM mode: fixed 4GB buffer at every capacity

8x
less DRAM at 32TB (32GB → 4GB)

32x
less DRAM at 128TB (128GB → 4GB)

Full map assumes 4KB IU and 32-bit PPA (FADU example, p.11). Reduced DRAM mode uses a fixed 4GB buffer at all capacities.
[1]TrendForce contract price surveys (Feb, Mar 2026). [2]TrendForce spot price, DDR5 16Gb (Oct 2026). [3]TrendForce, CSP capex and LTA terms (Aug 2026).

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Impact (2/2) – Three Biggest Risks We Face

Worst case: the controller supports DDR5 only

1 DDR5 cannot be sourced	2 LPDDR5X only, no DDR5	3 DDR5 nears end of life
• SSD vendors buy outside LTAs and get DDR5 last (Trend 2/4) • HBM + server RDIMM take 51% of 2026 DRAM bits[3]	• Some customers can secure LPDDR5X but not DDR5 • A DDR5-only controller cannot use that supply	• DDR6 commercial shipments expected 2028–29[1]; SK hynix roadmap 2029–30[2] • DDR5 output then shrinks, as DDR4 did in 2025–26
→ No DDR5, no SSD	**→ DRAM in hand, still no SSD**	**→ DDR5 gets scarcer every year**

Direction: need less DRAM, and accept either type

Reduce DRAM per drive: a smaller buffer cuts exposure to DRAM price and allocation

Support DDR5 and LPDDR5X: each customer builds with whichever DRAM it can buy

[1]TrendForce citing The Elec (May 2026). [2]SK hynix roadmap, SK AI Summit (Nov 2025). [3]TrendForce, CSP capex and LTA terms (Aug 2026).

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Decision (1/3) – Reduced DRAM, Sized from 4GB to 32GB

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Three options at 32TB (TLC, OP 7%), checked against the Gen6/7 targets: performance, power, endurance and DRAM supply

	Full DRAM	Reduced DRAM (Gen7)	DRAMless (Gen7)
DRAM size	32GB (1GB per TB)	Flexible 4–32GB (4GB minimum)	None
Where the map lives	Whole map in DRAM	Index in DRAM, full map in NAND	Whole map in NAND
Performance (Random Read)	Gen6: 6.8MIOPS (I/F Max) Gen7: 15MIOPS (I/F Max)	7~9MIOPS (Extra NAND read when map miss)	**6.8MIOPS (Gen6 I/F max)**
Power (Random Read)	Gen6: 23W @ 6.8MIOPS Gen7: <30W(TBD) @ 15MIOPS	<30W max @ 7~9MIOPS (within Gen6 budget)	<30W @ 6.8MIOPS
Power model (Only NAND Side)	15MIOPS * TLC tR power	7~9MIOPS * (TLC tR power + map miss rate * SLC tR Power)	6.8MIOPS * (TLC tR Power + SLC tR Power)
Endurance (≥1 DWPD)	1.687 DWPD	1.283 DWPD	**Below 1 DWPD (Critical)**
DRAM supply risk	**High**	Low	None
Decision	**Keep as Conventional mode**	**Selected ✓**	**Dropped**

Why Reduced DRAM: 4GB already clears 1 DWPD; DRAM can scale up to 32GB for performance

Red text: misses a target. FADU estimates (M1 4KiB IU on NAND, M2 512B IU in DRAM; Gen6 + BiCS8 power baseline). DRAMless endurance is a FADU assessment, not a modeled figure.

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Decision (2/3) – Gen7 Controller Targets the Gen6 Market

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PCIe generation mix in enterprise SSD exabytes shipped: Gen7 passes 50% only in CY32

Reference (p.9)	Full DRAM	Reduced DRAM (Gen7)	DRAMless (Gen7)
Performance (Ran. Read)	Gen6: 6.8MIOPS (I/F Max); Gen7: 15MIOPS (I/F Max)	7~9MIOPS (Extra NAND read when map miss)	**6.8MIOPS (Gen6 I/F max)**
Power (Ran. Read)	Gen6: 23W @ 6.8MIOPS; Gen7: <30W(TBD) @ 15MIOPS	<30W max @ 7~9MIOPS (within Gen6 budget)	<30W @ 6.8MIOPS
Endurance (≥1 DWPD)	1.687 DWPD	1.283 DWPD	**Below 1 DWPD (Critical)**

PCIe generation transitions, % of EB

PCIe gen	CY25	CY26	CY27	CY28	CY29	CY30	CY31	CY32
Gen 3.0	2%	1%						
Gen 4.0	70%	36%	17%	8%	4%	1%		
Gen 5.0	28%	60%	71%	61%	41%	31%	14%	7%
Gen 6.0		3%	12%	31%	**53%**	**57%**	**58%**	36%
Gen 7.0					**2%**	**11%**	28%	57%

Pink: Gen5/Gen6 CY29–CY32, the Reduced DRAM window. Red: early Gen7 volume.

What each segment needs

Gen6 and below

Reduced DRAM or DRAMless fits

Target Gen6 performance and latency for volume

Takeaway: Gen6 is 53–58% of EB in CY29–CY31, so a Reduced DRAM controller aimed at Gen6 covers the volume; Gen7 adds a cost-driven segment

Source: industry presentation “One Path to Cover the Market” (EB share by PCIe generation, CY25–CY32 forecast). Enzo: target reference performance named in the source.

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Decision (3/3) – Dual IP with LPDDR to Avoid DDR5 EOL Risk

THE PROBLEM

- FADU controller supports DDR5 only.
- Gen7 SSD market deployment window: 2030–2035.
- DDR5 EOL / supply risk in that window → no fallback today.

Gen7 SSD Lifecycle

	PCIe Spec. out	Gen3(2010)				Gen4		Gen5			Gen6			Gen7			Gen8(Est)																		
	Chip-out							Gen3		Gen4		Gen5			Gen6		Gen7(Est)		Gen8(Est)																
	SSD Drive (shipping)													Gen5			Gen6			Gen7(Est)			Gen8(Est)											
	Intel/AMD CPU											Gen5				Gen6		Gen7(Est)		Gen8(Est)														
	nVidia GPU										Gen5				Gen6		Gen7(Est)	Gen8(Est)																	
TSMC Node SNPS IP Available	DRAM	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039						
N12,28	LPDDR4			Spec	S6	S7							EOL																						
N7,12	LPDDR4X						S8(Spe	S9	S10																										
N5,7,12	LPDDR5								Spec	S20	S21	S22						EOL(Est)																
N3,5	LPDDR5X										Spec		S23	S24	S25	S26					EOL(Est)														
N2,3,4,5,6	LPDDR6														Spec			S27(Est)																	
	LPDDR6X																	Spec(Est)																	
N5,7,12	DDR4			5th	6th	7th	8th	9th		10th	11th					EOL																		
N3,5,7,12	DDR5										12th	13th	14th	UC2	UC2+	UC3(Est)							EOL(Est)											
N2,3	DDR6																	N2P, DDR6-c		S30(Est)														
	Memory Vendor Node						1x	1y		1z	1a		1b			1c		1d																	

Exhibit: DRAM & PCIe roadmap — DDR5 EOL est. ~2033 vs. Gen7 deploy window (red box)

*The schedule impact is limited to DRAM-related items only.

Option	Approach	Condition/Risk
A. Stay DDR5-only	DDR5 IP only	Fully exposed to DDR5 EOL / supply risk in 2030–2035
B. Move to DDR6	Replace DDR5 → DDR6	DDR6 spec finalizes ~end-2026; Synopsys IP on N2P (2nm) ships ~2028/Q1
C. Dual IP Selected ✓	DDR5 + LPDDR6(+5/5x)	Avoids EOL risk; LPDDR6 IP also covers LPDDR5/5x, expanding DRAM options

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Challenges – One Controller, Two Modes at Gen7 Speed

Where FADU engineering is focused now: one controller for both modes, and Gen7 performance without full DRAM

01

One controller, both modes

Conventional ↔ Reduced DRAM / DRAMless on the same silicon

DESIGN CONSTRAINTS

No damage to Conventional
Reduced DRAM support must not degrade the Conventional IO / data path

Theoretical performance
Reduced DRAM mode must reach its theoretical performance

No extra SRAM
Reduced DRAM must not add SRAM

02

Gen7 full performance in Reduced DRAM mode

Random read is bound by NAND ↔ controller IO

NAND IO TRAFFIC PER HOST RANDOM READ



Illustrative: a map miss adds a map page transfer on the same NAND channel

Current status
NAND IO 4,800MT/s + SCA still falls short of Gen7 random read

What else can close the gap?
How to reduce the count and size of map reads?

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